Netra t 1120/1125 Service Manual

THE NETWORK IS THE COMPUTER™

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Preface

The Netra t 1120/1125 *Service Manual* provides detailed procedures for the removal and replacement of field-replaceable parts in the XL (order code N04) and an XL (order code N03).

Note – This Guide does not apply to the version of XL supplied as order code N02.

Note – All illustrations in this manual are of the Netra t 1125, except where the two types of system differ, in which case examples of both are shown.

Who Should Use This Guide

This book is written for technicians, advanced computer system end-users with experience in replacing hardware and troubleshooting, system administrators and authorized service providers (ASPs). Only suitably-qualified service personnel may carry out the tasks described in this manual where they involve removal of access panels or the top cover.

How This Guide Is Organized

The guide is arranged as follows:

Chapter 1, “Description”, provides information on system features and components.

Chapter 2, “SunVTS Overview”, contains an overview of the Netra t 1120/1125 SunVTS diagnostic tool.

Chapter 3, “Power-On Self-Test”, contains procedures to initiate power-on self-test diagnostics.

Chapter 4, “Troubleshooting Procedures”, describes how to troubleshoot possible problems and includes suggested corrective actions.

Chapter 5, “Tool Requirements”, provides a description of the tools required.

Chapter 6, “Power On and Off”, contains procedures to power on and power off the Netra t 1120/1125.

Chapter 7, “Internal Access”, contains procedures to remove the Netra t 1120/1125’s top access cover, attach the wrist strap, and replace the top access cover.

Chapter 8, “Power Subassemblies”, contains procedures to remove and replace the power-related subassemblies of the Netra t 1120/1125.

Chapter 9, “Storage Devices”, contains procedures to remove and replace the storage devices.

Chapter 10, “Motherboard and Component Replacement”, contains removal and replacement procedures for the motherboard and components of the motherboard.

Appendix A, “Illustrated Parts List”, lists the authorized replaceable parts for the Netra t 1120/1125. A brief description of each listed component is also provided.

Appendix B, “Product Specifications”, provides physical, electrical and environmental specifications for the Netra t 1120/1125.

Appendix C, “Signal Descriptions”, gives signal descriptions for the motherboard connectors.

Related Documentation

- Netra t 1120/1125 Compliance and Safety Manual (805-6806-10)

Note – It is important that you read the Netra t 1120/1125 *Compliance and Safety Manual* before doing anything else.

- Netra t 1120/1125 Installation and Basic Maintenance Guide (805-6803-10)
- Netra t 1120/1125 System Reference Guide (805-6805-10)
- Netra t 1120/1125 User’s Guide (805-6802-10)

Conventions used in this Guide

The following table shows the type changes and symbols used in this guide.

TABLE P-1 Typographic Conventions

Typeface or Symbol	Meaning	Example
`AaBbCc123`	The names of commands, files, and directories; on-screen computer output	Edit your `.login` file. Use `ls -a` to list all files. `system% You have mail.`
`AaBbCc123`	What you type, as opposed to on-screen computer output	`system% su` `Password:`
AaBbCc123	Command-line placeholder: replace with a real name or value	To delete a file, type `rm` *filename*`.`
AaBbCc123	Book titles, new words or terms, or words to be emphasized	Read Chapter 6 in *User's Guide.* These are called *class* options. You *must* be root to do this.
%	UNIX C shell prompt	`system%`
$	UNIX Bourne and Korn shell prompt	`system$`
#	super-user prompt, all shells	`system#`

Symbols

The following symbols mean:

Note – A note provides information which should be considered by the reader.

Caution – Cautions accompanied by this Attention icon carry information about procedures or events which if not considered may cause damage to the data or hardware of your system.

Caution – Cautions accompanied by this Hazard icon carry information about procedures which must be followed to reduce the risk of electric shock and danger to personal health. Follow all instructions carefully.

1125 Paragraphs accompanied by this 1125 icon apply only to Netra t 1125 systems.

1120 Paragraphs accompanied by this 1120 icon apply only to Netra t 1120 systems.

Do Not Substitute Parts or Modify Equipment

Because of the danger of introducing additional hazards and/or the possibility of compromising emissions compliance, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local support organization for service and repair to ensure that safety features are maintained.

Placement of a Sun Product

Caution – To ensure reliable operation of the Sun product and to protect it from overheating, openings in the equipment must not be blocked or covered.

Power Connection

Caution – The system ON/STBY switch of this product functions as a standby type device only. The AC power connector or the external AC circuit breaker, if fitted, serves as the primary disconnect device for the system. It must be ensured that these remain accessible after installation or servicing.

Electrostatic Discharge

Caution – The boards and hard disk drives contain electronic components that are extremely sensitive to static electricity. Ordinary amounts of static electricity from clothes or work environment can destroy components.
Do not touch the components themselves or any metal parts. Wear a wrist strap when handling the drive assemblies, boards or cards.

Lithium Battery

Caution – On Sun system boards, a lithium battery is molded into the real-time clock, SDS No. M48T59Y, MK48TXXB-XX, M48T18-XXXPCZ or M48T59W-XXXPCZ.

Caution – Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

CHAPTER 1

Description

The Netra t 1120/1125 system uses the family of UltraSPARC™ II processors. Housed within a rack-mounting enclosure, the Netra t 1120/1125 provides the following:

- One or two UltraSPARC II processors
- Power and cooling for high performance processors
- Extensive I/O expansion and a wide range of options
- Modular internal design
- High performance disk, system, memory and I/O subsystem
- High-performance peripheral component interconnect (PCI) I/O expansion with comparable options to existing SBus options.

The Netra t 1120 is a –48V/–60Vdc-powered system. The Netra t 1125 is an AC-powered system. This is the only difference between the two systems.

FIGURE 1-2 and FIGURE 1-4 show front and rear views of the Netra t 1120/1125 system.

1.1 System Features

System components are housed in a rack-mounting enclosure. Overall enclosure dimensions (width x depth x height) are 431.8mm x 496.1mm x 177mm (17in x 19.53in x 7in (4U)). System electronics are contained on a single printed circuit board (motherboard). The motherboard contains the CPU module(s), memory, system control application-specific integrated circuits (ASICs) and I/O ASICs.

The system has the following features:

- Rack-mounting enclosure with power supply.
- Support for modular UltraSPARC II processor(s) with 1, 2 or 4 Mbyte Ecache, and system operating frequencies from 300MHz to 400MHz.
- UPA coherent memory interconnect.

- Use of SIMMs, with an interleaved memory system. Each pair of SIMM slots (four rows of two pairs each) accepts 32, 64 or 128Mbyte SIMM modules. Populating with two pairs of identical capacity SIMMs enables the memory controller to interleave and overlap, providing optimal system performance. There are a total of 16 SIMM slots.
- Four PCI slots:
  - Three 33MHz, 64- or 32-bit, 5Vdc slots
  - One 66MHz or 33MHz, 64- or 32-bit, 3.3Vdc slot.

  Universal PCI cards can be used in any of the four PCI slots.
- 10/100megabit per second (Mbps) Ethernet.
- Dual channel 40Mbps UltraSCSI (Fast-20).
- Two DB-25 serial ports (synchronous and asynchronous protocols).
- One parallel port.

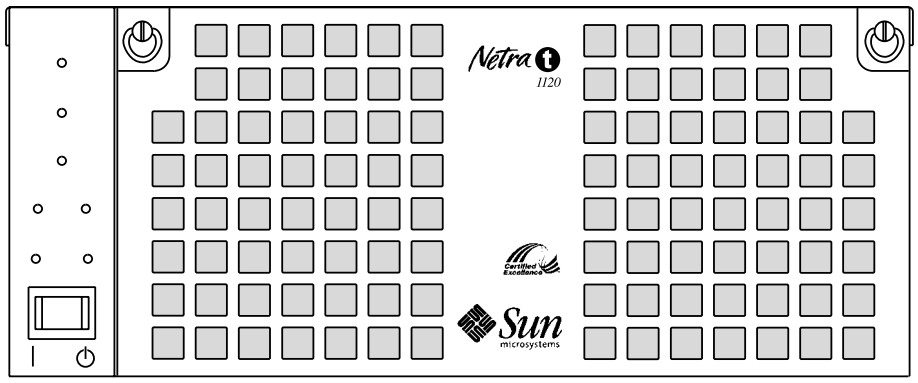


FIGURE 1-1 Netra t 1120 System Unit Front View

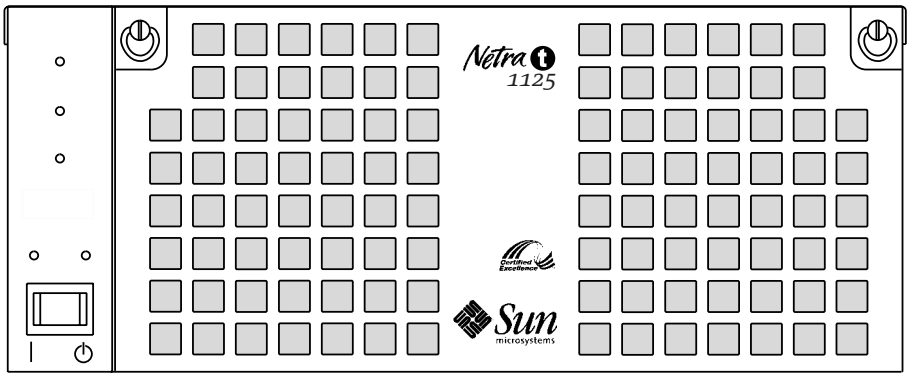


FIGURE 1-2 Netra t 1125 System Unit Front View

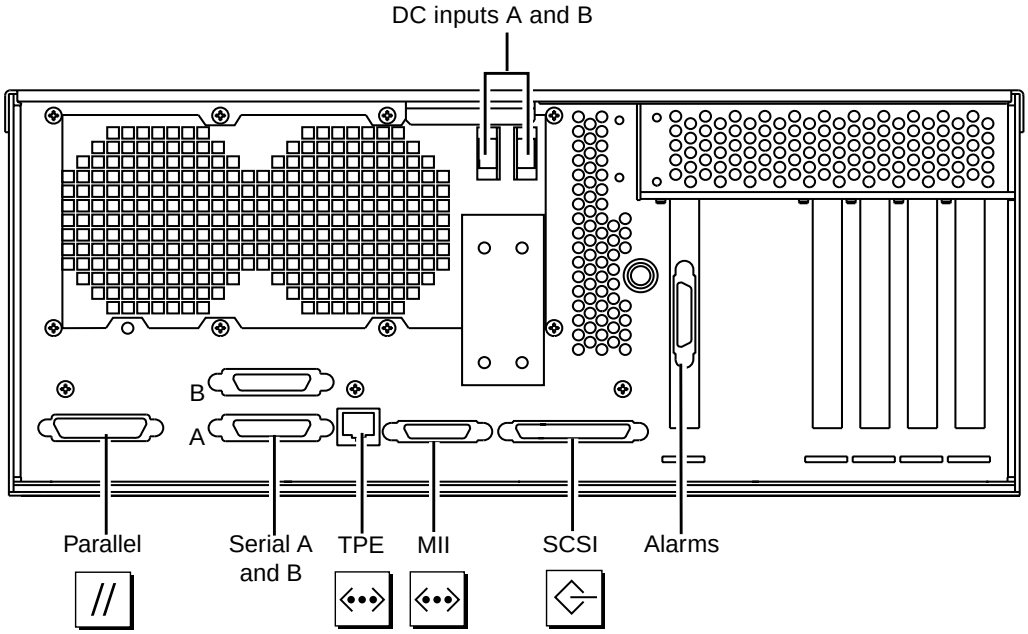


FIGURE 1-3 Netra t 1120 System Unit Rear View

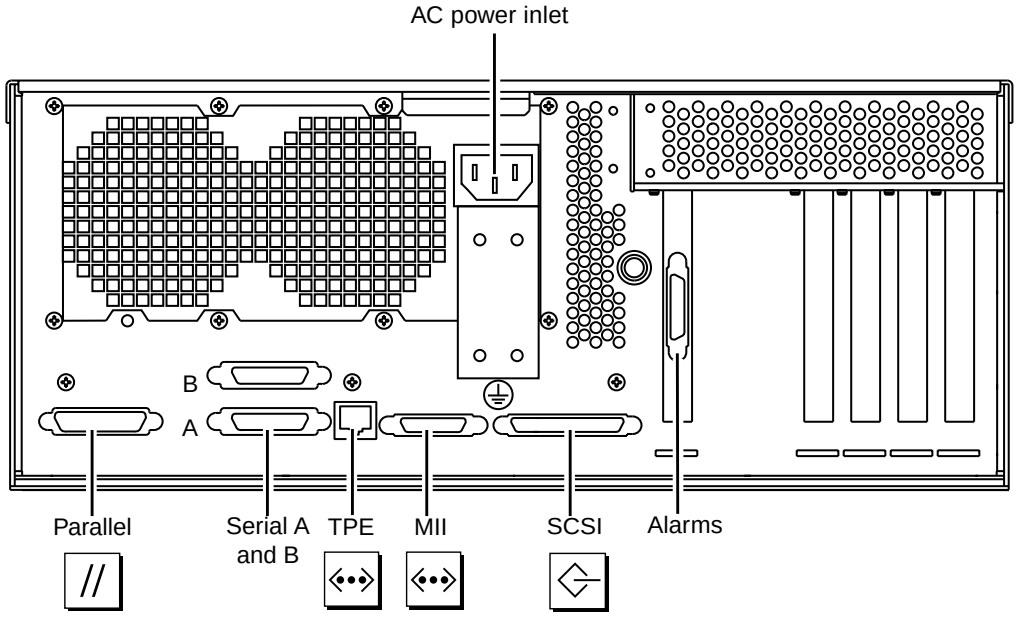
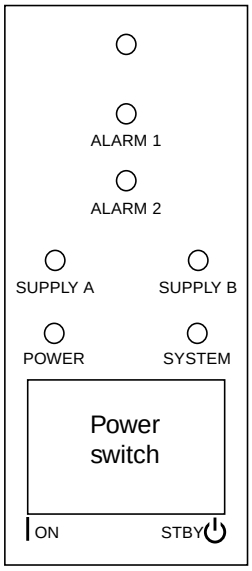


FIGURE 1-4 Netra t 1125 System Unit Rear View

1.2 System LEDs

1.2.1 Netra t 1120

The front panel has seven LEDs:



POWER–*Green*
This indicator is illuminated at all times when the system is On.

SUPPLY A–*Green*
Illuminated whenever DC input A is present and the system is powered on.

SUPPLY B–*Green*
Illuminated whenever DC input B is present and the system is powered on.

SYSTEM–*Green*
This indicator is off (or reset) during power up procedures and is illuminated whenever UNIX is running and the alarms driver is installed. It is reset by a hardware Watchdog timeout or, alternatively, whenever the user-defined Alarm 3 is asserted.

ALARM 1–*Amber*
Illuminated whenever the user-defined Alarm 1 is asserted.

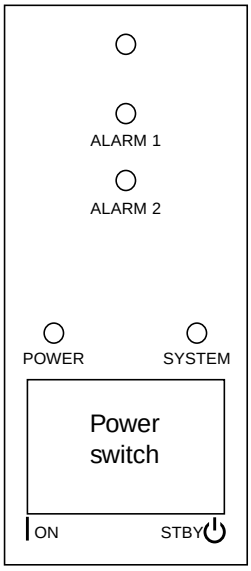
ALARM 2–*Amber*
Illuminated whenever the user-defined Alarm 2 is asserted.

SPARE–*Amber*
For future enhancement.

FIGURE 1-5 *Netra t 1120* System LEDs

1.2.2 Netra t 1125

The front panel has five LEDs:



POWER–*Green*
This indicator is illuminated at all times when the system is On.

SYSTEM–*Green*
This indicator is off (or reset) during power up procedures and is illuminated whenever UNIX is running and the alarms driver is installed. It is reset by a hardware Watchdog timeout or, alternatively, whenever the user-defined Alarm 3 is asserted.

ALARM 1–*Amber*
Illuminated whenever the user-defined Alarm 1 is asserted.

ALARM 2–*Amber*
Illuminated whenever the user-defined Alarm 2 is asserted.

SPARE–*Amber*
For future enhancement.

FIGURE 1-6 Netra t 1125 System LEDs

1.3 System Unit Components

TABLE A-1 on page A-3 lists the system unit components by part number. A brief description of each listed component is also provided.

Note – Part numbers listed in TABLE A-1 on page A-3 are correct as of the *Service Manual* publication date but are subject to change without notice. Consult your authorized Sun sales representative or service provider to confirm a part number prior to ordering a replacement part.

CHAPTER 2

SunVTS Overview

This chapter contains an overview of the Netra t 1120/1125 SunVTS™ diagnostic tool.

2.1 SunVTS Description

The SunVTS software executes multiple diagnostic hardware tests from a single user interface. SunVTS verifies the configuration, functionality and reliability of most hardware controllers and devices.

2.2 SunVTS Operation

TABLE 2-1 lists the documentation for the SunVTS software. These documents are available on the *Solaris on Sun Hardware AnswerBook*, which is on the *SMCC Updates CD-ROM* for the Solaris release.

TABLE 2-1 SunVTS Documentation

Title	Description
SunVTS User's Guide	Describes the SunVTS environment; starting and controlling various user interfaces; feature descriptions
SunVTS Test Reference Manual	Describes each SunVTS test; provides various test options and command line arguments
SunVTS Quick Reference Card	Provides overview of `vtsui` interface features

CHAPTER 3

Power-On Self-Test

This chapter contains procedures to initiate the Netra t 1120/1125 system unit power-on self-test (POST) diagnostics. Procedures are also included to support pre-POST preparation, POST data interpretation and the bypassing of POST diagnostics.

3.1 POST Overview

POST can be used to determine if part of the system unit has failed and should be replaced. POST detects approximately 95 percent of system unit faults, and is located in the system board OpenBoot™ PROM (OBP). The setting of two NVRAM variables, the `diag-switch?` and `diag-level` flags, determines if POST is executed. TABLE 3-1 lists the `diag-switch?` and `diag-level` flag settings for disabling POST (`off`), enabling POST maximum (`max`), or enabling POST minimum (`min`).

TABLE 3-1 `diag-Level` Switch Settings

`Diag-Level` **Setting**	**POST Initialization**	**Serial Port A IO**	**Serial Port A Error Output**	`diag-Switch?` **Setting**
Off	No	N/A	N/A	N/A
Max	Yes (power-on)	Enabled	Enabled	True
Min	Yes (power-on)	Disabled	Enabled	True

3.2 Pre-POST Preparation

Pre-POST preparation includes:

- Setting up a `tip` connection to another workstation or terminal to view POST progress and error messages. See Section 3.2.1 “To Set Up a `tip` Connection below.
- Verifying baud rates between a Netra t 1120/1125 and a terminal. See Section 3.2.2 “To Verify the Baud Rate” on page 3-3.

3.2.1 To Set Up a `tip` Connection

A `tip` connection enables a remote shell window to be used as a terminal to display test data from a system being tested. Serial ports A or B are used to establish the `tip` connection between the system unit being tested and another Sun workstation monitor or TTY-type terminal. The `tip` connection is used in a SunOS window and provides features to help with the OBP.

1. **Connect serial port A of the system being tested to another Sun workstation serial port B using a serial null modem cable (connect cable pins 2-3, 3-2, 7-20, and 20-7).**
2. **At the other Sun workstation, check the `/etc/remote` file:**

```
hardwire:\
    :dv=/dev/term/b:br#9600:el=^C^S^Q^U^D:ie=%$:oe=^D:
```

Note – The example shows connection to serial port B, `ttyb`.

3. **To use serial port A:**
   a. **Copy and paste the following:**

```
hardwire:\
    :dv=/dev/term/b:br#9600:el=^C^S^Q^U^D:ie=%$:oe=^D:
```

b. Then modify as follows:

```
hardwire:\
    :dv=/dev/term/a:br#9600:el=^C^S^Q^U^D:ie=%$:oe=^D:
```

4. **In a Shell Tool window on the Sun workstation, type `tip hardwire`. Verify the response:**

```
hostname% tip hardwire
connected
```

Note – The shell window is now a `tip` window directed to the serial port of the system unit being tested. When power is applied to the system unit being tested, POST messages will be displayed in this window.

---

5. **When POST is completed, disconnect the `tip` window by typing `~.` (tilde+period).**

3.2.2 To Verify the Baud Rate

To verify the baud rate between the system unit being tested and a terminal or another Sun workstation monitor:

1. **Open a Shell Tool.**
2. **Type `eeprom`.**
3. **Verify the following serial port default settings as follows:**

```
ttyb-mode = 9600,8,n,1
ttya-mode = 9600,8,n,1
```

Note – Ensure that the settings are consistent with TTY-type terminal or workstation monitor settings.

3.3 To Initialize POST

POST is initialized by setting `diag-switch?` to `true` and `diag-level` to `max` or `min`, followed by power cycling the system unit.

1. **At the system prompt, type:**

```
setenv diag-switch? true
```

2. **When the POST is complete, set `diag-switch?` to `false` (default setting).**

3.4 Maximum and Minimum Levels of POST

Two levels of POST are available: maximum (`max`) level and minimum (`min`) level. The system initiates the selected level of POST based on the setting of `diag-level`, an NVRAM variable.

The default setting for `diag-level` is `max`. An example of a `max` level POST output on serial port A is provided in Section 3.4.1 “`diag-level` Variable Set to `max`” on page 3-5. An example of a `min` level POST output on serial port A is provided in Section 3.4.2 “`diag-level` Variable Set to `min`” on page 3-14.

To set `diag-level` to `min`, type:

```
ok setenv diag-level min
```

To return to the default setting:

```
ok setenv diag-level max
```

3.4.1 `diag-level` Variable Set to `max`

When the `diag-level` variable is set to `max`, POST enables an extended set of diagnostic-level tests. This mode requires approximately four and a half minutes to complete. CODE EXAMPLE 3-1 identifies a typical serial port A POST output with `diag-level` set to `max`.

Note – xxxx placeholders used in table entries represent numeric values which can change without notice.

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max`

```
Hardware Power ON

Master CPU online
Master Version: 0000.0000.1700.1120
Slave  Version: 0000.0000.1700.1120
CPU E$ (M) 0000.0000.0020.0000 (S) 0000.0000.0020.0000Button Power
ON

Master CPU online
Master Version: 0000.0000.1700.1120
Slave  Version: 0000.0000.1700.1120
CPU E$ (M) 0000.0000.0020.0000 (S) 0000.0000.0020.0000

Probing keyboard Done
%o0 = 0000.0000.0000.4001

Executing Power On SelfTest

0>
0>@(#) Sun Ultra 60(UltraSPARC-II 2-way) UPA/PCI POST 1.0.8 01/21/
1998 02:36 PM
0>INFO: Processor 0 is master.
0>
0> <00> Init System BSS
0> <00> NVRAM Battery Detect Test
0> <00> NVRAM Scratch Addr Test
0> <00> DMMU TLB Tag Access Test
0> <00> DMMU TLB RAM Access Test
0> <00> IMMU TLB Tag Access Test
0> <00> IMMU TLB RAM Access Test
0> <00> Probe Ecache
0>INFO: CPU 296 MHz: 2048KB Ecache
0> <00> Ecache RAM Addr Test
0> <00> Ecache Tag Addr Test
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` *(Continued)*

```
 0> <00> Ecache Tag Test
 0> <00> Invalidate Ecache Tags
 0>INFO: Processor 2 - UltraSPARC-II.
 0> <00> Init SC Regs
 0> <00> SC Address Reg Test
 0> <00> SC Reg Index Test
 0> <00> SC Regs Test
 0> <00> SC Dtag RAM Addr Test
 0> <00> SC Cache Size Init
 0> <00> SC Dtag RAM Data Test
 0> <00> SC Dtag Init
 0> <00> Probe Memory
 0>INFO:   0MB Bank 0
 0>INFO:   0MB Bank 1
 0>INFO:   0MB Bank 2
 0>INFO: 128MB Bank 3
 0> <00> Malloc Post Memory
 0> <00> Init Post Memory
 0> <00> Post Memory Addr Test
 0> <00> Map PROM/STACK/NVRAM in DMMU
 0> <00> Memory Stack Test
 2> <00> DMMU TLB Tag Access Test
 2> <00> DMMU TLB RAM Access Test
 2> <00> IMMU TLB Tag Access Test
 2> <00> IMMU TLB RAM Access Test
 2> <00> Probe Ecache
 2>INFO: CPU 296 MHz: 2048KB Ecache
 2> <00> Ecache RAM Addr Test
 2> <00> Ecache Tag Addr Test
 2> <00> Ecache Tag Test
 2> <00> Invalidate Ecache Tags
 2> <00> Map PROM/STACK/NVRAM in DMMU
 2> <00> Update Slave Stack/Frame Ptrs
 0> <00> DMMU Hit/Miss Test
 0> <00> IMMU Hit/Miss Test
 0> <00> DMMU Little Endian Test
 0> <00> IU ASI Access Test
 0> <00> FPU ASI Access Test
 2> <00> DMMU Hit/Miss Test
 2> <00> IMMU Hit/Miss Test
 2> <00> DMMU Little Endian Test
 2> <00> IU ASI Access Test
 2> <00> FPU ASI Access Test
 2> <00> Dcache RAM Test
 2> <00> Dcache Tag Test
 2> <00> Icache RAM Test
 2> <00> Icache Tag Test
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` *(Continued)*

```
 2> <00> Icache Next Test
 2> <00> Icache Predecode Test
 0> <1f> Init Psycho
 0> <1f> PIO Read Error, Master Abort Test
 0> <1f> PIO Read Error, Target Abort Test
 0> <1f> PIO Write Error, Master Abort Test
 0> <1f> PIO Write Error, Target Abort Test
 0> <1f> Timer Increment Test
 0> <1f> Consistent DMA UE ECC Rd Err Lpbk Test
 0> <1f> Pass-Thru DMA UE ECC Rd Err Lpbk Test
 0> <00> Copy Post to Memory
 0> <00> Ecache Thrash Test
 0> <00> Init Memory
 0> <00> Memory Addr w/ Ecache Test
 0>INFO:   0MB Bank 0
 0>INFO:   0MB Bank 1
 0>INFO:   0MB Bank 2
 0>INFO: 128MB Bank 3
 0> <00> Block Memory Addr Test
 0>INFO:   0MB Bank 0
 0>INFO:   0MB Bank 1
 0>INFO:   0MB Bank 2
 0>INFO: 128MB Bank 3
 0> <00> ECC Memory Addr Test
 0>INFO:   0MB Bank 0
 0>INFO:   0MB Bank 1
 0>INFO:   0MB Bank 2
 0>INFO: 128MB Bank 3
 0> <00> Memory Status Test
 0>INFO:   0MB Bank 0
 0>INFO:   0MB Bank 1
 0>INFO:   0MB Bank 2
 0>INFO: 128MB Bank 3
 0> <00> V9 Instruction Test
 0> <00> CPU Tick and Tick Compare Reg Test
 0> <00> CPU Soft Trap Test
 0> <00> CPU Softint Reg and Int Test
 2> <00> V9 Instruction Test
 2> <00> CPU Tick and Tick Compare Reg Test
 0> <1f> Init Psycho
 0> <1f> Psycho Cntl and UPA Reg Test
 0> <1f> Psycho DMA Scoreboard Reg Test
 0> <1f> Psycho Perf Cntl Reg Test
 0> <1f> PIO Decoder and BCT Test
 0> <1f> PCI Byte Enable Test
 0> <1f> Counter/Timer Limit Regs Test
 0> <1f> Timer Reload Test
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` *(Continued)*

```
 0> <1f> Timer Periodic Test
 0> <1f> Mondo Int Map (short) Reg Test
 0> <1f> Mondo Int Set/Clr Reg Test
 0> <1f> Psycho IOMMU Regs Test
 0> <1f> Psycho IOMMU RAM Address Test
 0> <1f> Psycho IOMMU CAM Address Test
 0> <1f> IOMMU TLB Compare Test
 0> <1f> IOMMU TLB Flush Test
 0> <1f> Stream Buff A Control Reg Test
 0> <1f> Psycho ScacheA Page Tag Addr Test
 0> <1f> Psycho ScacheA Line Tag Addr Test
 0> <1f> Psycho ScacheA RAM Addr Test
 0> <1f> Psycho ScacheA Error Status NTA Test
 0> <1f> Psycho ScacheB Page Tag Addr Test
 0> <1f> Psycho ScacheB Line Tag Addr Test
 0> <1f> Psycho ScacheB RAM Addr Test
 0> <1f> Psycho ScacheB Error Status NTA Test
 0> <1f> PBMA PCI Config Space Regs Test
 0> <1f> PBMA Control/Status Reg Test
 0> <1f> PBMA Diag Reg Test
 0> <1f> PBMB PCI Config Space Regs Test
 0> <1f> PBMB Control/Status Reg Test
 0> <1f> PBMB Diag Reg Test
 0> <00> FPU Regs Test
 0> <00> FPU Move Regs Test
 0> <00> FPU State Reg Test
 0> <00> FPU Functional Test
 0> <00> FPU Trap Test
 0> <00> DMMU Primary Context Reg Test
 0> <00> DMMU Secondary Context Reg Test
 0> <00> DMMU TSB Reg Test
 0> <00> DMMU Tag Access Reg Test
 0> <00> DMMU VA Watchpoint Reg Test
 0> <00> DMMU PA Watchpoint Reg Test
 0> <00> IMMU TSB Reg Test
 0> <00> IMMU Tag Access Reg Test
 0> <00> DMMU TLB Tag Access Test
 0> <00> DMMU TLB RAM Access Test
 0> <00> Dcache RAM Test
 0> <00> Dcache Tag Test
 0> <00> Icache RAM Test
 0> <00> Icache Tag Test
 0> <00> Icache Next Test
 0> <00> Icache Predecode Test
 2> <00> FPU Regs Test
 2> <00> FPU Move Regs Test
 2> <00> FPU State Reg Test
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` *(Continued)*

```
 2> <00> FPU Functional Test
 2> <00> FPU Trap Test
 2> <00> DMMU Primary Context Reg Test
 2> <00> DMMU Secondary Context Reg Test
 2> <00> DMMU TSB Reg Test
 2> <00> DMMU Tag Access Reg Test
 2> <00> DMMU VA Watchpoint Reg Test
 2> <00> DMMU PA Watchpoint Reg Test
 2> <00> IMMU TSB Reg Test
 2> <00> IMMU Tag Access Reg Test
 2> <00> DMMU TLB Tag Access Test
 2> <00> DMMU TLB RAM Access Test
 0> <00> CPU Addr Align Trap Test
 0> <00> DMMU Access Priv Page Test
 0> <00> DMMU Write Protected Page Test
 0> <1f> Init Psycho
 0> <1f> Pri CE ECC Error Test
 0> <1f> Pri UE ECC Error Test
 0> <1f> Pri 2 bit w/ bit hole UE ECC Err Test
 0> <1f> Pri 3 bit UE ECC Err Test
 0> <1f> Streaming DMA UE ECC Rd Err Ebus Test
 0> <1f> Streaming DMA CE ECC Rd Err Ebus Test
 0> <1f> Streaming DMA CE ECC Rd Err Lpbk Test
 0> <1f> Consistent DMA UE ECC Rd Error Ebus Test
 0> <1f> Consistent DMA UE ECC R/M/W Err Ebus Test
 0> <1f> Consistent DMA UE ECC R/M/W Err Lpbk Test
 0> <1f> Consistent DMA CE ECC Rd Err Ebus Test
 0> <1f> Consistent DMA CE ECC Rd Err Lpbk Test
 0> <1f> Consistent DMA CE ECC R/M/W Err Ebus Test
 0> <1f> Consistent DMA CE ECC R/M/W Err Lpbk Test
 0> <1f> Consistent DMA Wr Data Parity Err Lpbk Test
 0> <1f> Pass-Thru DMA UE ECC Rd Err Ebus Test
 0> <1f> Pass-Thru DMA UE ECC R/M/W Err Ebus Test
 0> <1f> Pass-Thru DMA UE ECC R/M/W Err Lpbk Test
 0> <1f> Pass-Thru DMA CE ECC Rd Err Ebus Test
 0> <1f> Pass-Thru DMA CE ECC Rd Err Lpbk Test
 0> <1f> Pass-Thru DMA CE ECC R/M/W Err Ebus Test
 0> <1f> Pass-Thru DMA CE ECC R/M/W Err Lpbk Test
 0> <1f> Pass-Thru DMA Write Data Parity Err, Lpbk Test
 0> <1f> Init Psycho
 0> <1f> Mondo Generate Interrupt Test
 0> <1f> Timer Interrupt Test
 0> <1f> Timer Interrupt w/ periodic Test
 0> <1f> Psycho Stream Buff A Flush Sync Test
 0> <1f> Psycho Stream Buff B Flush Sync Test
 0> <1f> Psycho Stream Buff A Flush Invalidate Test
 0> <1f> Psycho Stream Buff B Flush Invalidate Test
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` *(Continued)*

```
 0> <1f> Psycho Merge Buffer w/ Scache A Test
 0> <1f> Psycho Merge Buffer w/ Scache B Test
 0> <1f> Consist DMA Rd, IOMMU miss Ebus Test
 0> <1f> Consist DMA Rd, IOMMU miss Lpbk Test
 0> <1f> Consist DMA Rd, IOMMU hit Ebus Test
 0> <1f> Consist DMA Rd, IOMMU hit Lpbk Test
 0> <1f> Consist DMA Wr, IOMMU miss Ebus Test
 0> <1f> Consist DMA Wr, IOMMU miss Lpbk Test
 0> <1f> Consist DMA Wr, IOMMU hit Ebus Test
 0> <1f> Consist DMA Wr, IOMMU hit Lpbk Test
 0> <1f> Stream DMA Rd, IOMMU miss, Scache Miss Ebus Test
 0> <1f> Stream DMA Rd, IOMMU miss, Scache Miss Lpbk Test
 0> <1f> Stream DMA Rd, IOMMU hit, Scache Miss Ebus Test
 0> <1f> Stream DMA Rd, IOMMU hit, Scache Miss Lpbk Test
 0> <1f> Stream DMA Rd, IOMMU Miss, Scache(prev rd) Hit Ebus Test
 0> <1f> Stream DMA Rd, IOMMU Miss, Scache Hit (prev rd) Lpbk Test
 0> <1f> Stream DMA Rd, IOMMU Hit, Scache Hit Ebus Test
 0> <1f> Stream DMA Rd, IOMMU Hit, Scache Hit (prev rd) Lpbk Test
 0> <1f> Stream DMA Rd, IOMMU Miss, Scache Hit(prev wr) Ebus Test
 0> <1f> Stream DMA Rd, IOMMU Miss, Scache Hit (prev wr) Lpbk Test
 0> <1f> Stream DMA Rd, IOMMU Hit, Scache Hit(prev wr) Ebus Test
 0> <1f> Stream DMA Rd, IOMMU Hit, Scache Hit (prev wr) Lpbk Test
 0> <1f> Stream DMA Wr, IOMMU miss, Scache Miss Ebus Test
 0> <1f> Stream DMA Wr, IOMMU miss, Scache Miss Lpbk Test
 0> <1f> Stream DMA Wr, IOMMU hit, Scache Miss Ebus Test
 0> <1f> Stream DMA Wr, IOMMU hit, Scache Miss Lpbk Test
 0> <1f> Stream DMA Wr, IOMMU Miss, Scache(prev rd) Hit Ebus Test
 0> <1f> Stream DMA Wr, IOMMU Miss, Scache(prev rd) Hit Lpbk Test
 0> <1f> Stream DMA Wr, IOMMU Hit, Scache(prev rd) Hit Ebus Test
 0> <1f> Stream DMA Wr, IOMMU Hit, Scache(prev rd) Hit Lpbk Test
 0> <1f> Stream DMA Wr, IOMMU Miss, Scache(prev wr) Hit Ebus Test
 0> <1f> Stream DMA Wr, IOMMU Miss, Scache(prev wr) Hit Lpbk Test
 0> <1f> Stream DMA Wr, IOMMU Hit, Scache(prev wr) Hit Ebus Test
 0> <1f> Stream DMA Wr, IOMMU Hit, Scache(prev wr) Hit Lpbk Test
 0> <1f> Pass-Thru DMA Rd, Ebus device Test
 0> <1f> Pass-Thru DMA Rd, Loopback Mode Test
 0> <1f> Pass-Thru DMA Wr, Ebus device Test
 0> <1f> Pass-Thru DMA Wr, Loopback Mode Test
 0> <1f> Consist DMA Rd, IOMMU LRU Lock Ebus Test
 0> <1f> Consist DMA Rd, IOMMU LRU Lock Lpbk Test
 0> <1f> Stream DMA Rd, IOMMU LRU Lock, Scache LRU Lock Ebus Test
 0> <1f> Stream DMA Rd, IOMMU LRU Lock, Scache LRU Lock Lpbk Test
 0> <1f> Stream DMA Rd, IOMMU miss, Scache LRU Lock Ebus Test
 0> <1f> Stream DMA Rd, IOMMU Miss, Scache LRU Lock Lpbk Test
 0> <1f> Stream DMA Rd, IOMMU Hit, Scache LRU Lock Ebus Test
 0> <1f> Stream DMA Rd, IOMMU Hit, Scache LRU Lock Lpbk Test
 0> <1f> Stream DMA Rd, IOMMU LRU Lock, Scache Miss Ebus Test
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` *(Continued)*

```
 0> <1f> Stream DMA Rd, IOMMU LRU Lock, Scache Miss Lpbk Test
 0> <1f> Consist DMA Wr, IOMMU LRU Locked Ebus Test
 0> <1f> Consist DMA Wr, IOMMU LRU Lock Lpbk Test
 0> <1f> Stream DMA Wr, IOMMU LRU Lock, Scache LRU Lock Ebus Test
 0> <1f> Stream DMA Wr, IOMMU LRU Lock, Scache LRU Lock Lpbk Test
 0> <1f> Stream DMA Wr, IOMMU Miss, Scache LRU Lock Ebus Test
 0> <1f> Stream DMA Wr, IOMMU Miss, Scache LRU Lock Lpbk Test
 0> <1f> Stream DMA Wr, IOMMU Hit, Scache LRU Lock Ebus Test
 0> <1f> Stream DMA Wr, IOMMU Hit, Scache LRU Lock Lpbk Test
 0> <1f> Stream DMA Wr, IOMMU LRU Lock, Scache Miss Ebus Test
 0> <1f> Stream DMA Wr, IOMMU LRU Lock, Scache Miss Lpbk Test
 0> <1f> Stream DMA Wr, IOMMU LRU Lock, Scache(prev rd) Hit Ebus
Test
 0> <1f> Stream DMA Wr, IOMMU LRU Lock, Scache(prev rd) Hit Lpbk
Test
 0> <00> Init Memory
 0>INFO:   0MB Bank 0
 0>INFO:   0MB Bank 1
 0>INFO:   0MB Bank 2
 0>INFO: 128MB Bank 3
 0> <00> Memory w/ Ecache Test
 0>INFO:   0MB Bank 0
 0>INFO:   0MB Bank 1
 0>INFO:   0MB Bank 2
 0>INFO: 128MB Bank 3
 0> <00> Block Memory Test
 0>INFO:   0MB Bank 0
 0>INFO:   0MB Bank 1
 0>INFO:   0MB Bank 2
 0>INFO: 128MB Bank 3
 0> <00> ECC Blk Memory Test
 0>INFO:   0MB Bank 0
 0>INFO:   0MB Bank 1
 0>INFO:   0MB Bank 2
 0>INFO: 128MB Bank 3
 0> <00> UltraSPARC-2 Prefetch Instructions Test
 0> <00> Test 0: prefetch_mr
 0> <00> Test 1: prefetch to non-cacheable page
 0> <00> Test 2: prefetch to page with dmmu misss
 0> <00> Test 3: prefetch miss does not check alignment
 0> <00> Test 4: prefetcha with asi 0x4c is noped
 0> <00> Test 5: prefetcha with asi 0x54 is noped
 0> <00> Test 6: prefetcha with asi 0x6e is noped
 0> <00> Test 7: prefetcha with asi 0x76 is noped
 0> <00> Test 8: prefetch with fcn 5
 0> <00> Test 9: prefetch with fcn 2
 0> <00> Test 10: prefetch with fcn 12
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` *(Continued)*

```
 0> <00> Test 11: prefetch with fcn 16 is noped
 0> <00> Test 12: prefetch with fcn 29 is noped
 0> <00> Test 13: prefetcha with asi 0x15 is noped
 0> <00> Test 14: prefetch with fcn 3
 0> <00> Test 15: prefetcha14 with fcn 2
 0> <00> Test 16: prefetcha80_mr
 0> <00> Test 17: prefetcha81_1r
 0> <00> Test 18: prefetcha10_mw
 0> <00> Test 19: prefetcha80_17 is noped
 0> <00> Test 20: prefetcha10_6: illegal instruction trap
 0> <00> Test 21: prefetcha11_1w
 0> <00> Test 22: prefetcha81_31
 0> <00> Test 23: prefetcha11_15: illegal instruction trap
 2> <00> UltraSPARC-2 Prefetch Instructions Test
 2> <00> Test 0: prefetch_mr
 2> <00> Test 1: prefetch to non-cacheable page
 2> <00> Test 2: prefetch to page with dmmu misss
 2> <00> Test 3: prefetch miss does not check alignment
 2> <00> Test 4: prefetcha with asi 0x4c is noped
 2> <00> Test 5: prefetcha with asi 0x54 is noped
 2> <00> Test 6: prefetcha with asi 0x6e is noped
 2> <00> Test 7: prefetcha with asi 0x76 is noped
 2> <00> Test 8: prefetch with fcn 5
 2> <00> Test 9: prefetch with fcn 2
 2> <00> Test 10: prefetch with fcn 12
 2> <00> Test 11: prefetch with fcn 16 is noped
 2> <00> Test 12: prefetch with fcn 29 is noped
 2> <00> Test 13: prefetcha with asi 0x15 is noped
 2> <00> Test 14: prefetch with fcn 3
 2> <00> Test 15: prefetcha14 with fcn 2
 2> <00> Test 16: prefetcha80_mr
 2> <00> Test 17: prefetcha81_1r
 2> <00> Test 18: prefetcha10_mw
 2> <00> Test 19: prefetcha80_17 is noped
 2> <00> Test 20: prefetcha10_6: illegal instruction trap
 2> <00> Test 21: prefetcha11_1w
 2> <00> Test 22: prefetcha81_31
 2> <00> Test 23: prefetcha11_15: illegal instruction trap
 0>STATUS =PASSED


 Power On Selftest Completed
 ~Software Power ON.0000.0000.0000 ffff.ffff.f00b.3110
 ff9f.ffff.0bd1.1111

 Master CPU online
 Master Version: 0000.0000.1700.1120
```

CODE EXAMPLE 3-1 diag-level Variable Set to max *(Continued)*

```
Slave  Version: 0000.0000.1700.1120
CPU E$ (M) 0000.0000.0020.0000 (S) 0000.0000.0020.0000

@(#) Sun Ultra 60 UPA/PCI  3.11 Version 25 created 1998/01/16 12:22
Clearing DTAGS  Done
Probing Memory Done
MEM BASE = 0000.0000.a000.0000
MEM SIZE = 0000.0000.0800.0000
MMUs ON
Copy Done
PC = 0000.01ff.f000.27e0
PC = 0000.0000.0000.2824
Decompressing into Memory Done
Size = 0000.0000.0006.e820
ttya initialized
SC Control: EWP:0 IAP:0 FATAL:0 WAKEUP:0 BXIR:0 BPOR:0 SXIR:0
SPOR:1 POR:0
Probing Memory Bank #0   0   0   0   0 :   0 Megabytes
Probing Memory Bank #1   0   0   0   0 :   0 Megabytes
Probing Memory Bank #2   0   0   0   0 :   0 Megabytes
Probing Memory Bank #3  32  32  32  32 : 128 Megabytes
Probing Floppy: No drives detected
Probing EBUS SUNW,tsalarm
Probing UPA Slot at 1e,0 Nothing there
Probing UPA Slot at 1d,0 Nothing there
Probing /pci@1f,4000 at Device 1  pci108e,1000 network
Probing /pci@1f,4000 at Device 3  scsi disk tape scsi disk tape
Probing /pci@1f,4000 at Device 2  Nothing there
Probing /pci@1f,4000 at Device 4  Nothing there
Probing /pci@1f,4000 at Device 5  Nothing there
Probing /pci@1f,2000 at Device 1  Nothing there
Probing /pci@1f,2000 at Device 2  Nothing there
screen not found.
Can't open input device.
Keyboard not present.  Using ttya for input and output.
SC Control: EWP:0 IAP:0 FATAL:0 WAKEUP:0 BXIR:0 BPOR:0 SXIR:0
SPOR:1 POR:0
Probing Memory Bank #0   0   0   0   0 :   0 Megabytes
Probing Memory Bank #1   0   0   0   0 :   0 Megabytes
Probing Memory Bank #2   0   0   0   0 :   0 Megabytes
Probing Memory Bank #3  32  32  32  32 : 128 Megabytes
Probing Floppy: No drives detected
Probing EBUS SUNW,tsalarm
Probing UPA Slot at 1e,0 Nothing there
Probing UPA Slot at 1d,0 Nothing there
Probing /pci@1f,4000 at Device 1  pci108e,1000 network
Probing /pci@1f,4000 at Device 3  scsi disk tape scsi disk tape
```

CODE EXAMPLE 3-1 `diag-level` Variable Set to `max` *(Continued)*

```
Probing /pci@1f,4000 at Device 2  Nothing there
Probing /pci@1f,4000 at Device 4  Nothing there
Probing /pci@1f,4000 at Device 5  Nothing there
Probing /pci@1f,2000 at Device 1  Nothing there
Probing /pci@1f,2000 at Device 2  Nothing there

Sun Ultra 60 UPA/PCI (2 X UltraSPARC-II 296MHz), No Keyboard
OpenBoot 3.11, 128 MB memory installed, Serial #9637699.
Ethernet address 8:0:20:93:f:43, Host ID: 80930f43.
```

3.4.2 `diag-level` Variable Set to `min`

When `diag-level` is set to `min`, POST enables an abbreviated set of diagnostic-level tests. This mode requires approximately three minutes to complete. CODE EXAMPLE 3-2 identifies a serial port A POST output with `diag-level` set to `min`.

CODE EXAMPLE 3-2 `diag-level` Variable Set to `min`

```
Hardware Power ON

Master CPU online
Master Version: 0000.0000.1700.1120
Slave  Version: 0000.0000.1700.1120
CPU E$ (M) 0000.0000.0020.0000 (S) 0000.0000.0020.0000Button Power
ON

Master CPU online
Master Version: 0000.0000.1700.1120
Slave  Version: 0000.0000.1700.1120
CPU E$ (M) 0000.0000.0020.0000 (S) 0000.0000.0020.0000

Probing keyboard Done
%o0 = 0000.0000.0000.2001

Executing Power On SelfTest

0>
0>@(#) Sun Ultra 60(UltraSPARC-II 2-way) UPA/PCI POST 1.0.8 01/21/
1998 02:36 PM
0>INFO: Processor 0 is master.
0>
0> <00> Init System BSS
0> <00> NVRAM Battery Detect Test
0> <00> NVRAM Scratch Addr Test
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `min` *(Continued)*

```
 0> <00> DMMU TLB Tag Access Test
 0> <00> DMMU TLB RAM Access Test
 0> <00> IMMU TLB Tag Access Test
 0> <00> IMMU TLB RAM Access Test
 0> <00> Probe Ecache
 0>INFO: CPU 296 MHz: 2048KB Ecache
 0> <00> Ecache RAM Addr Test
 0> <00> Ecache Tag Addr Test
 0> <00> Ecache Tag Test
 0> <00> Invalidate Ecache Tags
 0>INFO: Processor 2 - UltraSPARC-II.
 0> <00> Init SC Regs
 0> <00> SC Address Reg Test
 0> <00> SC Reg Index Test
 0> <00> SC Regs Test
 0> <00> SC Dtag RAM Addr Test
 0> <00> SC Cache Size Init
 0> <00> SC Dtag RAM Data Test
 0> <00> SC Dtag Init
 0> <00> Probe Memory
 0>INFO:   0MB Bank 0
 0>INFO:   0MB Bank 1
 0>INFO:   0MB Bank 2
 0>INFO: 128MB Bank 3
 0> <00> Malloc Post Memory
 0> <00> Init Post Memory
 0> <00> Post Memory Addr Test
 0> <00> Map PROM/STACK/NVRAM in DMMU
 0> <00> Memory Stack Test
 2> <00> DMMU TLB Tag Access Test
 2> <00> DMMU TLB RAM Access Test
 2> <00> IMMU TLB Tag Access Test
 2> <00> IMMU TLB RAM Access Test
 2> <00> Probe Ecache
 2>INFO: CPU 296 MHz: 2048KB Ecache
 2> <00> Ecache RAM Addr Test
 2> <00> Ecache Tag Addr Test
 2> <00> Ecache Tag Test
 2> <00> Invalidate Ecache Tags
 2> <00> Map PROM/STACK/NVRAM in DMMU
 2> <00> Update Slave Stack/Frame Ptrs
 0> <00> DMMU Hit/Miss Test
 0> <00> IMMU Hit/Miss Test
 0> <00> DMMU Little Endian Test
 0> <00> IU ASI Access Test
 0> <00> FPU ASI Access Test
 2> <00> DMMU Hit/Miss Test
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `min` *(Continued)*

```
2> <00> IMMU Hit/Miss Test
2> <00> DMMU Little Endian Test
2> <00> IU ASI Access Test
2> <00> FPU ASI Access Test
2> <00> Dcache RAM Test
2> <00> Dcache Tag Test
2> <00> Icache RAM Test
2> <00> Icache Tag Test
2> <00> Icache Next Test
2> <00> Icache Predecode Test
0> <1f> Init Psycho
0> <1f> PIO Read Error, Master Abort Test
0> <1f> PIO Read Error, Target Abort Test
0> <1f> PIO Write Error, Master Abort Test
0> <1f> PIO Write Error, Target Abort Test
0> <1f> Timer Increment Test
0> <1f> Consistent DMA UE ECC Rd Err Lpbk Test
0> <1f> Pass-Thru DMA UE ECC Rd Err Lpbk Test
0> <00> Copy Post to Memory
0> <00> Ecache Thrash Test
0> <00> Init Memory
0> <00> Memory Addr w/ Ecache Test
0>INFO:   0MB Bank 0
0>INFO:   0MB Bank 1
0>INFO:   0MB Bank 2
0>INFO: 128MB Bank 3
0> <00> Block Memory Addr Test
0>INFO:   0MB Bank 0
0>INFO:   0MB Bank 1
0>INFO:   0MB Bank 2
0>INFO: 128MB Bank 3
0> <00> ECC Memory Addr Test
0>INFO:   0MB Bank 0
0>INFO:   0MB Bank 1
0>INFO:   0MB Bank 2
0>INFO: 128MB Bank 3
0> <00> Memory Status Test
0>INFO:   0MB Bank 0
0>INFO:   0MB Bank 1
0>INFO:   0MB Bank 2
0>INFO: 128MB Bank 3
0> <00> V9 Instruction Test
0> <00> CPU Tick and Tick Compare Reg Test
0> <00> CPU Soft Trap Test
0> <00> CPU Softint Reg and Int Test
2> <00> V9 Instruction Test
2> <00> CPU Tick and Tick Compare Reg Test
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `min` *(Continued)*

```
0> <1f> Init Psycho
0> <1f> Psycho Cntl and UPA Reg Test
0> <1f> Psycho DMA Scoreboard Reg Test
0> <1f> Psycho Perf Cntl Reg Test
0> <1f> PIO Decoder and BCT Test
0> <1f> PCI Byte Enable Test
0> <1f> Counter/Timer Limit Regs Test
0> <1f> Timer Reload Test
0> <1f> Timer Periodic Test
0> <1f> Mondo Int Map (short) Reg Test
0> <1f> Mondo Int Set/Clr Reg Test
0> <1f> Psycho IOMMU Regs Test
0> <1f> Psycho IOMMU RAM Address Test
0> <1f> Psycho IOMMU CAM Address Test
0> <1f> IOMMU TLB Compare Test
0> <1f> IOMMU TLB Flush Test
0> <1f> Stream Buff A Control Reg Test
0> <1f> Psycho ScacheA Page Tag Addr Test
0> <1f> Psycho ScacheA Line Tag Addr Test
0> <1f> Psycho ScacheA RAM Addr Test
0> <1f> Psycho ScacheA Error Status NTA Test
0> <1f> Psycho ScacheB Page Tag Addr Test
0> <1f> Psycho ScacheB Line Tag Addr Test
0> <1f> Psycho ScacheB RAM Addr Test
0> <1f> Psycho ScacheB Error Status NTA Test
0> <1f> PBMA PCI Config Space Regs Test
0> <1f> PBMA Control/Status Reg Test
0> <1f> PBMA Diag Reg Test
0> <1f> PBMB PCI Config Space Regs Test
0> <1f> PBMB Control/Status Reg Test
0> <1f> PBMB Diag Reg Test
0> <00> UltraSPARC-2 Prefetch Instructions Test
0> <00> Test 0: prefetch_mr
0> <00> Test 1: prefetch to non-cacheable page
0> <00> Test 2: prefetch to page with dmmu misss
0> <00> Test 3: prefetch miss does not check alignment
0> <00> Test 4: prefetcha with asi 0x4c is noped
0> <00> Test 5: prefetcha with asi 0x54 is noped
0> <00> Test 6: prefetcha with asi 0x6e is noped
0> <00> Test 7: prefetcha with asi 0x76 is noped
0> <00> Test 8: prefetch with fcn 5
0> <00> Test 9: prefetch with fcn 2
0> <00> Test 10: prefetch with fcn 12
0> <00> Test 11: prefetch with fcn 16 is noped
0> <00> Test 12: prefetch with fcn 29 is noped
0> <00> Test 13: prefetcha with asi 0x15 is noped
0> <00> Test 14: prefetch with fcn 3
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `min` *(Continued)*

```
 0> <00> Test 15: prefetcha14 with fcn 2
 0> <00> Test 16: prefetcha80_mr
 0> <00> Test 17: prefetcha81_1r
 0> <00> Test 18: prefetcha10_mw
 0> <00> Test 19: prefetcha80_17 is noped
 0> <00> Test 20: prefetcha10_6: illegal instruction trap
 0> <00> Test 21: prefetcha11_1w
 0> <00> Test 22: prefetcha81_31
 0> <00> Test 23: prefetcha11_15: illegal instruction trap
 2> <00> UltraSPARC-2 Prefetch Instructions Test
 2> <00> Test 0: prefetch_mr
 2> <00> Test 1: prefetch to non-cacheable page
 2> <00> Test 2: prefetch to page with dmmu misss
 2> <00> Test 3: prefetch miss does not check alignment
 2> <00> Test 4: prefetcha with asi 0x4c is noped
 2> <00> Test 5: prefetcha with asi 0x54 is noped
 2> <00> Test 6: prefetcha with asi 0x6e is noped
 2> <00> Test 7: prefetcha with asi 0x76 is noped
 2> <00> Test 8: prefetch with fcn 5
 2> <00> Test 9: prefetch with fcn 2
 2> <00> Test 10: prefetch with fcn 12
 2> <00> Test 11: prefetch with fcn 16 is noped
 2> <00> Test 12: prefetch with fcn 29 is noped
 2> <00> Test 13: prefetcha with asi 0x15 is noped
 2> <00> Test 14: prefetch with fcn 3
 2> <00> Test 15: prefetcha14 with fcn 2
 2> <00> Test 16: prefetcha80_mr
 2> <00> Test 17: prefetcha81_1r
 2> <00> Test 18: prefetcha10_mw
 2> <00> Test 19: prefetcha80_17 is noped
 2> <00> Test 20: prefetcha10_6: illegal instruction trap
 2> <00> Test 21: prefetcha11_1w
 2> <00> Test 22: prefetcha81_31
 2> <00> Test 23: prefetcha11_15: illegal instruction trap
 0>STATUS =PASSED


 Power On Selftest Completed
 ~Software Power ON.0000.0000.0000 ffff.ffff.f00b.3110
 ff9f.ffff.0bd1.1111

 Master CPU online
 Master Version: 0000.0000.1700.1120
 Slave  Version: 0000.0000.1700.1120
 CPU E$ (M) 0000.0000.0020.0000 (S) 0000.0000.0020.0000

 @(#) Sun Ultra 60 UPA/PCI  3.11 Version 25 created 1998/01/16 12:22
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `min` *(Continued)*

```
Clearing DTAGS  Done
Probing Memory Done
MEM BASE = 0000.0000.a000.0000
MEM SIZE = 0000.0000.0800.0000
MMUs ON
Copy Done
PC = 0000.01ff.f000.27e0
PC = 0000.0000.0000.2824
Decompressing into Memory Done
Size = 0000.0000.0006.e820
ttya initialized
SC Control: EWP:0 IAP:0 FATAL:0 WAKEUP:0 BXIR:0 BPOR:0 SXIR:0
SPOR:1 POR:0
Probing Memory Bank #0   0   0   0   0 :   0 Megabytes
Probing Memory Bank #1   0   0   0   0 :   0 Megabytes
Probing Memory Bank #2   0   0   0   0 :   0 Megabytes
Probing Memory Bank #3  32  32  32  32 : 128 Megabytes
Probing Floppy: No drives detected
Probing EBUS SUNW,tsalarm
Probing UPA Slot at 1e,0 Nothing there
Probing UPA Slot at 1d,0 Nothing there
Probing /pci@1f,4000 at Device 1  pci108e,1000 network
Probing /pci@1f,4000 at Device 3  scsi disk tape scsi disk tape
Probing /pci@1f,4000 at Device 2  Nothing there
Probing /pci@1f,4000 at Device 4  Nothing there
Probing /pci@1f,4000 at Device 5  Nothing there
Probing /pci@1f,2000 at Device 1  Nothing there
Probing /pci@1f,2000 at Device 2  Nothing there
screen not found.
Can't open input device.
Keyboard not present.  Using ttya for input and output.
SC Control: EWP:0 IAP:0 FATAL:0 WAKEUP:0 BXIR:0 BPOR:0 SXIR:0
SPOR:1 POR:0
Probing Memory Bank #0   0   0   0   0 :   0 Megabytes
Probing Memory Bank #1   0   0   0   0 :   0 Megabytes
Probing Memory Bank #2   0   0   0   0 :   0 Megabytes
Probing Memory Bank #3  32  32  32  32 : 128 Megabytes
Probing Floppy: No drives detected
Probing EBUS SUNW,tsalarm
Probing UPA Slot at 1e,0 Nothing there
Probing UPA Slot at 1d,0 Nothing there
Probing /pci@1f,4000 at Device 1  pci108e,1000 network
Probing /pci@1f,4000 at Device 3  scsi disk tape scsi disk tape
Probing /pci@1f,4000 at Device 2  Nothing there
Probing /pci@1f,4000 at Device 4  Nothing there
Probing /pci@1f,4000 at Device 5  Nothing there
Probing /pci@1f,2000 at Device 1  Nothing there
```

CODE EXAMPLE 3-2 `diag-level` Variable Set to `min` *(Continued)*

```
Probing /pci@1f,2000 at Device 2  Nothing there

Sun Ultra 60 UPA/PCI (2 X UltraSPARC-II 296MHz), No Keyboard
OpenBoot 3.11, 128 MB memory installed, Serial #9637699.
Ethernet address 8:0:20:93:f:43, Host ID: 80930f43.
```

3.5 POST Progress and Error Reporting

While POST is initialized, POST progress indications are visible when a TTY-type terminal or a `tip` line is connected between serial port A (default port) of the system being tested and a POST monitoring system.

If an error occurs during execution, POST attempts to send a failure message to the POST monitoring system. CODE EXAMPLE 3-3 identifies the typical appearance of a failure message.

Note – The system does not automatically boot if a POST error occurs; it halts at the `ok` prompt to alert the user of a failure.

CODE EXAMPLE 3-3 Typical Error Code Failure Message

```
UltraSPARC-2 Prefetch Instructions Test
CPU UPA Config: 000006b8.3cc0803b
SRAM Mode: 22 Clock Mode: 3:1 ELIM: 4 PCON: 0f3 MCAP: 13
Ecache Size Limited: 2048KB
Test 0: prefetch_mr
STATUS =FAILED
TEST   =UltraSPARC-2 Prefetch Instructions
TTF    =0
PASSES =1
ERRORS =1
SUSPECT=CPU (Basic) U0101
MESSAGE=
Edata Mismatch(T0) Data compare error.
addr     00000000.40802000
expected 00000000
observed 22222222
xor      22222222
```

3.6 Motherboard Test

To initialize the motherboard POST:

1. **Either**:

   a. From a terminal connected to ttyA, issue a `break` command to enter OBP, or

   b. From a `tip` hardwire connection, send a `break` command.

2. **At the OK prompt, type**:

```
setenv diag-level max
setenv diag-switch? true
reset-all
```

The system will now reset and commence POST.

Note – Non-optional components, such as four SIMMs in slots U0701, U0801, U0901 and U1001, the motherboard, the power supply and the keyboard must be installed for POST to execute properly. Removing the optional system components and retesting the system isolates the possibility that those components are the cause of the failure.

CHAPTER 4

Troubleshooting Procedures

This chapter describes how to troubleshoot possible problems with the Netra t 1120/1125 system unit and includes suggested corrective actions. To follow these troubleshooting procedures, a terminal should be connected to the Netra t 1120/1125 system serial port A.

4.1 Power-On Failure

This section provides examples of power-on failure symptoms and suggested actions.

Symptom

The system does not power up when the power switch is pressed.

Action

Check that the input power connector(s) is / are correctly fitted. Check that the external circuit breaker(s), if fitted, is / are correctly set.

Press the power switch at the front of the system unit. If the system powers on, no further action is required. If the system does not power on, one of the CPU modules may not be properly seated. Remove the top cover and inspect each CPU module for proper seating. If the system powers on, no further action is required.

If the input power has been verified, each CPU module is properly seated, and the power-on key has been pressed but the system does not power up, the system power supply may be defective. See Section 4.3 “Power Supply Test” on page 4-5.

Symptom

The system attempts to power up but does not boot.

Action

Press the power-on button. If the system unit still fails to boot, refer to Section 3.6 “Motherboard Test” on page 3-22.

4.2 Disk Drive or Removable Media Drive Failure

This section provides disk drive and removable media drive failure symptoms and suggested actions.

Symptom

- A disk drive read, write or parity error is reported by the operating system or customer application.
- A removable media drive read error or parity error is reported by the operating system or customer application.

Action

- Replace the drive indicated by the failure message as described in Section 9.1 “Hard Disk Drive” on page 9-2. The operating system identifies the internal drives as identified in TABLE 4-1.

TABLE 4-1 Internal Drive Identification

Operating System Address	Drive Physical Location and Target
c0t0d0s#	Lower SCSI Disk, target 0
c0t1d0s#	Upper SCSI Disk, target 1 (optional)
c0t6d0s#	CD-ROM drive, target 6 (optional)
c0t5d0s#	Tape drive, target 5 (optional)

Note – The # symbol in the operating system address examples will be a numeral between 0 and 7 that describes the slice or partition on the drive.

Symptom

Disk drive or removable media drive fails to respond to commands.

Note – If POST is to be bypassed, type **`setenv diag-switch? false`** at the `ok` prompt.

Action

Test the drive response to the `probe-scsi` command as follows:

- **At the system `ok` prompt:**

  a. Type `reset-all`.

  b. Type `probe-scsi`.

  If the drives respond and a message is displayed, the system SCSI controller has successfully probed the devices. This indicates that the system board is operating correctly.

  If one drive does not respond to the SCSI controller probe but the others do, replace the unresponsive drive as described in Section 9.1 “Hard Disk Drive” on page 9-2 or Section 9.2 “Removable Media Drive” on page 9-5.

  If one internal disk drive is configured with the system and the `probe-scsi` test fails to show the device in the message, replace the drive as described in Section 9.1 “Hard Disk Drive” on page 9-2 or Section 9.2 “Removable Media Drive” on page 9-5.

  If the problem is still evident after replacing the drive, replace the SCSI backplane assembly as described in Section 9.3 “SCSI Backplane” on page 9-8.

  If replacing both the disk drive and the SCSI backplane assembly does not correct the problem, replace the motherboard as described in Section 10.7 “Motherboard” on page 10-24.

4.3 Power Supply Test

This section describes how to test the power supply. FIGURE 4-1 and TABLE 4-2 identify power supply connector J2901. FIGURE 4-2 and TABLE 4-3 identify power supply connector J2902. FIGURE 4-3 and TABLE 4-4 identify power supply connector J2903.

1. **Attach a wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the power cord(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Follow Step 4 to Step 9 in Section 8.1.1 “To Remove the Power Supply” on page 8-1.**

5. **Lift the power supply from the chassis until it is restrained by the power supply cables. Rest the power supply on the front crossmember of the enclosure to expose connectors J2901 through J2903.**

6. **Reconnect the input power connector(s) and power on the system.**

   See Section 6.1 “To Power On the System” on page 6-2.

7. **Using a digital voltage meter (DVM), check the power supply output voltages as follows:**

Note – Power supply connectors J2901 through J2903 must remain connected to the motherboard.

---

   a. **With the negative probe of the DVM placed on a connector ground (Gnd) pin, position the positive probe on each power pin.**

   b. **Verify voltage and signal availability as listed in the tables below.**

8. **If any power pin signal is not present with the power supply active and properly connected to the motherboard, replace the power supply.**

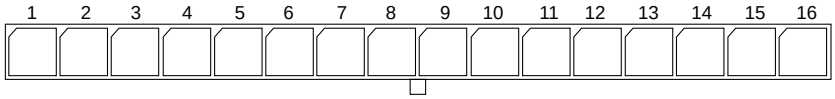


FIGURE 4-1 Power Supply Connector J2901

TABLE 4-2 Power Supply Connector J2901 Pin Description

Pin	Description	Pin	Description
1	Rtn	9	SUPPLY TRIP L
2	+3.3Vdc SENSE	10	POWERON L
3	Rtn	11	–12Vdc
4	+5.0Vdc SENSE	12	POWER OK
5	POWER SET0 NEG	13	Rtn
6	+3.0Vdc SENSE	14	+12Vdc
7	POWER 0V	15	Rtn
8	POWER SET0 POS	16	+12Vdc

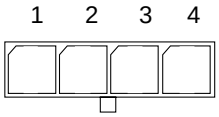


FIGURE 4-2 Power Supply Connector J2902

TABLE 4-3 Power Supply Connector J2902 Pin Description

Pin	Description	Pin	Description
1	+5.0Vdc Rtn	3	+3.0Vdc Rtn
2	+5.0Vdc	4	+3.0Vdc

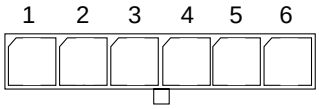


FIGURE 4-3 Power Supply Connector J2903

TABLE 4-4 Power Supply Connector J2903 Pin Description

Pin	Function	Pin	Function
1	+3.3Vdc Rtn	4	+3.3Vdc
2	+3.3Vdc Rtn	5	+3.3Vdc
3	+3.3Vdc Rtn	6	+3.3Vdc

4.4 SIMM Failure

At times, the operating system, diagnostic program or POST may not display a SIMM location (U number) as part of a memory error message. In this situation, the only available information is a physical memory address and failing byte (or bit). TABLE 4-5 lists physical memory addresses to locate a defective SIMM.

TABLE 4-5 SIMM Physical Memory Address

SIMM Slot	SIMM Pair (non-interleave)	SIMM Quad (interleave)
U701 U801	00000000 - 0fffffff	00000000 - 1fffffff
U901 U1001	10000000 - 1fffffff	
U702 U802	20000000 - 2fffffff	20000000 - 3fffffff
U902 U1002	30000000 - 3fffffff	
U703 U803	40000000 - 4fffffff	40000000 - 5fffffff
U903 U1003	50000000 - 5fffffff	
U704 U804	60000000 - 6fffffff	60000000 - 7fffffff
U904 U1004	70000000 - 7fffffff	

CHAPTER 5

Tool Requirements

This chapter lists the tools required to service the Netra t 1120/1125 system:

- No.1 and No.2 Phillips-head screwdriver
- Needle-nose pliers
- Antistatic wrist strap
- Digital voltage meter (DVM)
- Antistatic mat.

Place ESD-sensitive components such as system board, circuit cards, disk drives and NVRAM/TOD on an antistatic mat. The following items can be used as an antistatic mat:

- Bag used to wrap a Sun replacement part
- Shipping container used to package a Sun replacement part
- Inner side (metal part) of the system unit cover
- Sun ESD mat, part number 250-1088 (which can be purchased through your Sun sales representative)
- Disposable ESD mat; shipped with replacement parts or optional system features.

CHAPTER 6

Power On and Off

This chapter describes how to power on and power off the Netra t 1120/1125 system.

6.1 To Power On the System

1. **Turn on power to all connected peripherals.**

Note – Peripheral power is activated prior to system power so the system can recognize the peripherals when it is activated.

---

2. **Momentarily set the front panel ON/STBY system switch to the ON position (**FIGURE 6-1**).**

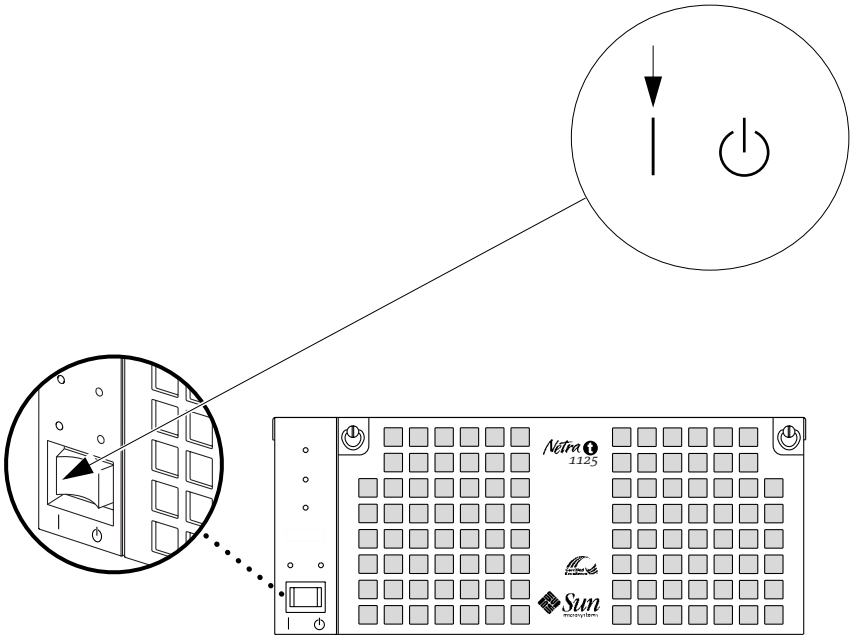


FIGURE 6-1 System Power-On (Front Panel)

6.2 To Power Off the System

Caution – Prior to turning off system power, exit from the operating system. Failure to do so may result in data loss.

1. **Where necessary, notify users that the system is going down.**
2. **Back up system files and data.**
3. **Halt the operating system.**
4. **Momentarily set the front panel ON/STBY system switch to the STBY position (**FIGURE 6-2**) until the system powers down.**
5. **Verify that the Power LED is off.**
6. **Disconnect the input power connector(s) on the rear of the unit, or open all circuit breakers associated with the unit.**

Caution –

1120 Regardless of the position of the ON/STBY switch, where a DC power cord remains connected to the system, DC voltage is always present within the power supply.

1125 Regardless of the position of the ON/STBY switch, where an AC power cord remains connected to the system, hazardous voltages are always present within the power supply.

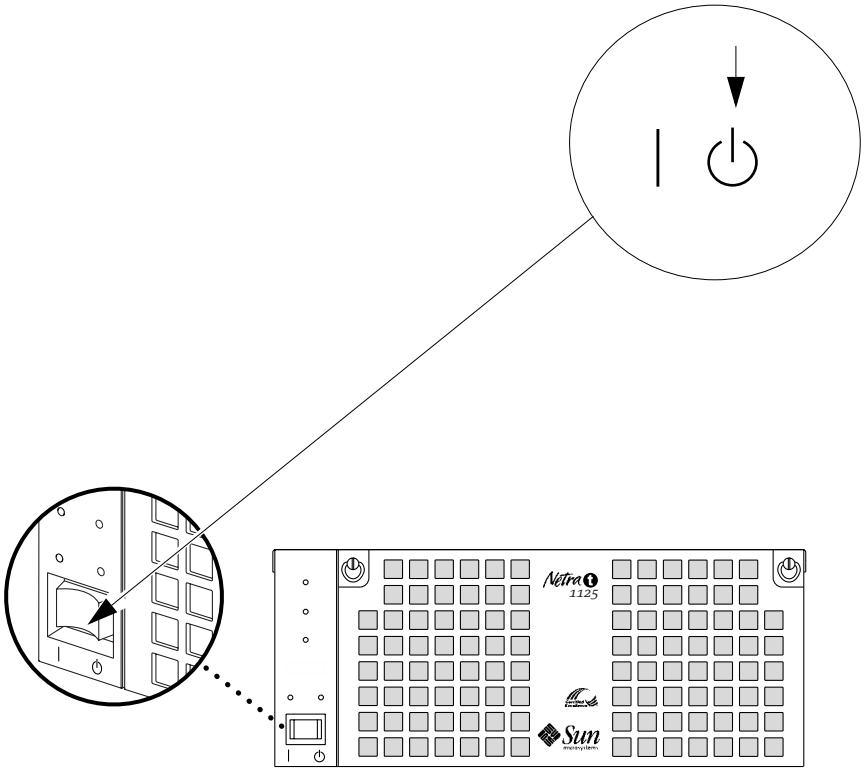


FIGURE 6-2 System Power-Off (Front Panel)

CHAPTER 7

Internal Access

This chapter contains procedures to attach the wrist strap and to remove and replace the system top access cover

7.1 To Attach the Wrist Strap

Caution – Wear an antistatic wrist strap and use an ESD-protected mat when handling components. When servicing or removing system unit components, use a wrist strap with a 10mm press stud connection and attach the wrist strap to the press stud at the front or rear of the chassis. This should be performed before the top cover is removed.

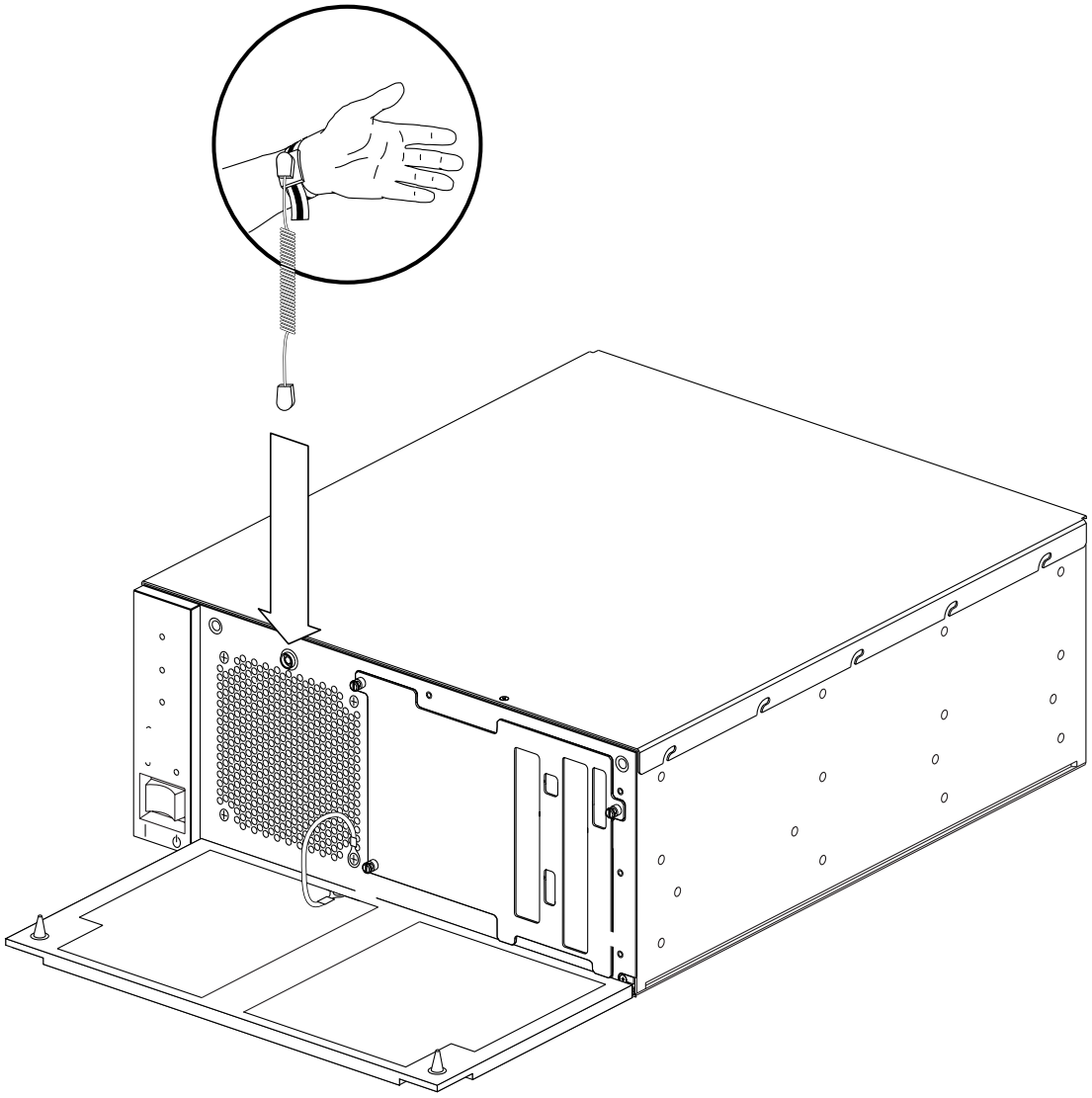


FIGURE 7-1 Attaching the Wrist Strap to the Front of the Chassis

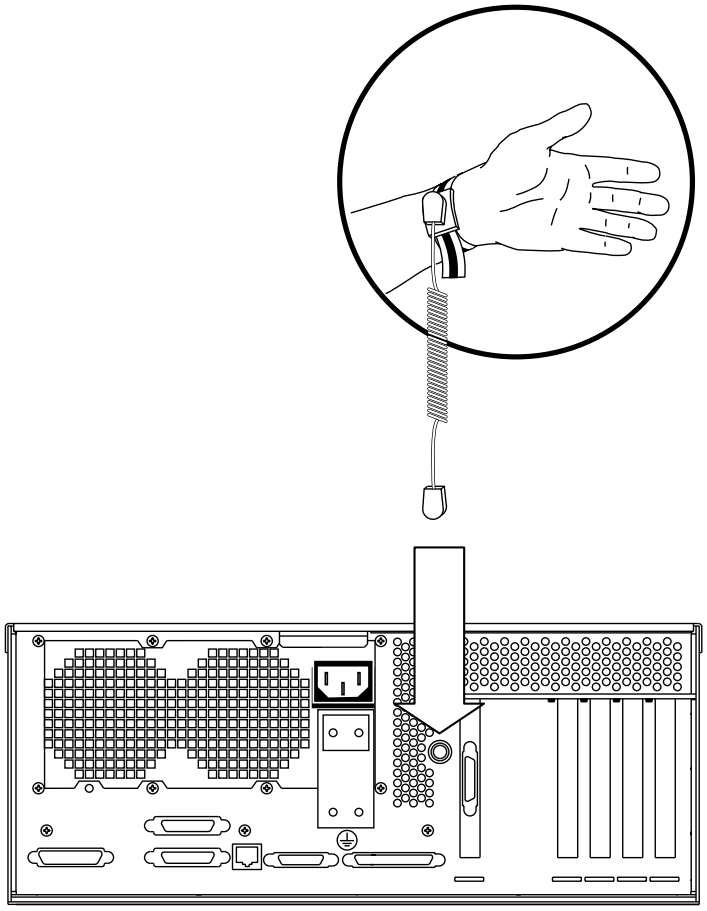


FIGURE 7-2 Attaching the Wrist Strap to the Rear of the Chassis

7.2 To Remove the Top Access Cover

Caution – Wear an antistatic wrist strap and use an ESD-protected mat when handling components. When servicing or removing system unit components, an ESD Strap should be attached to the wrist, then to one of the connection points provided on the system, and then the power connectors should be removed from the system unit. Following this caution equalizes all electrical potentials with the system unit.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system.**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Disconnect the input power connector(s).**

4. **Remove the rack fixing screws and withdraw the unit on its slides (if fitted).**

   To remove the top access cover, the unit may need to be completely removed from the rack. If slides are fitted, disconnect the cables and release the slides. Place the system on an approved work station / position.

5. **Remove the two screws from the front of the top access cover and carefully store them away from the system unit.**

6. **Refer to** FIGURE 7-3**. Place the system so that the extended tab of the top access cover is facing you. To release the top cover, pull the tab towards you and lift the cover off.**

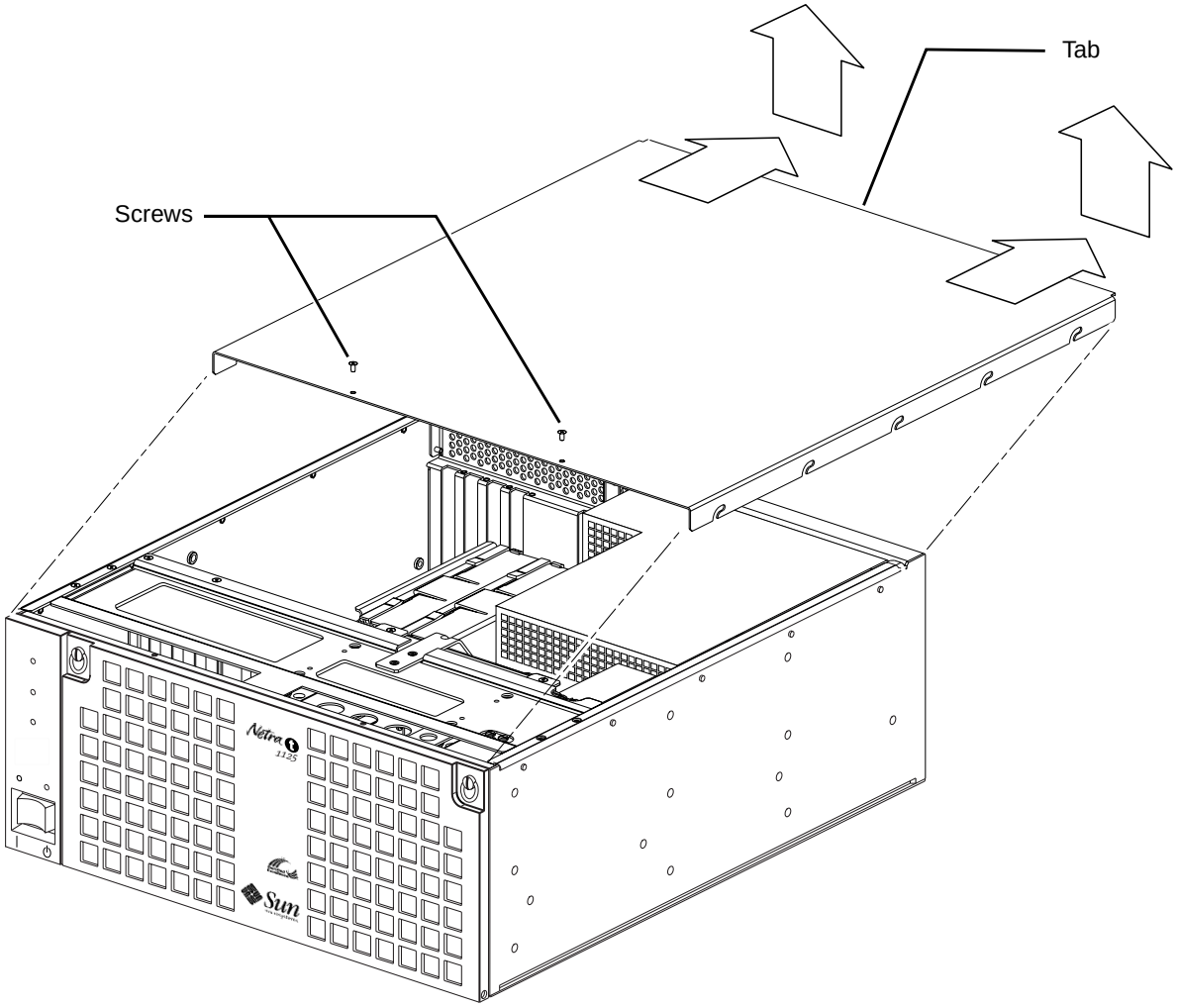


FIGURE 7-3 Removing the Top Access Cover

7.3 To Replace the Top Access Cover

Caution – Wear an antistatic wrist strap and use an ESD-protected mat when handling components. When servicing or removing system unit components, an ESD Strap should be attached to the wrist, then to one of the connection points provided on the system, and then the power connectors should be removed from the system unit.Following this caution equalizes all electrical potentials with the system unit.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Position the top access cover.**

   See FIGURE 7-4.

3. **Push the cover forwards until the lugs on the sides have fully engaged in the slots.**

4. Replace the two fixing screws.

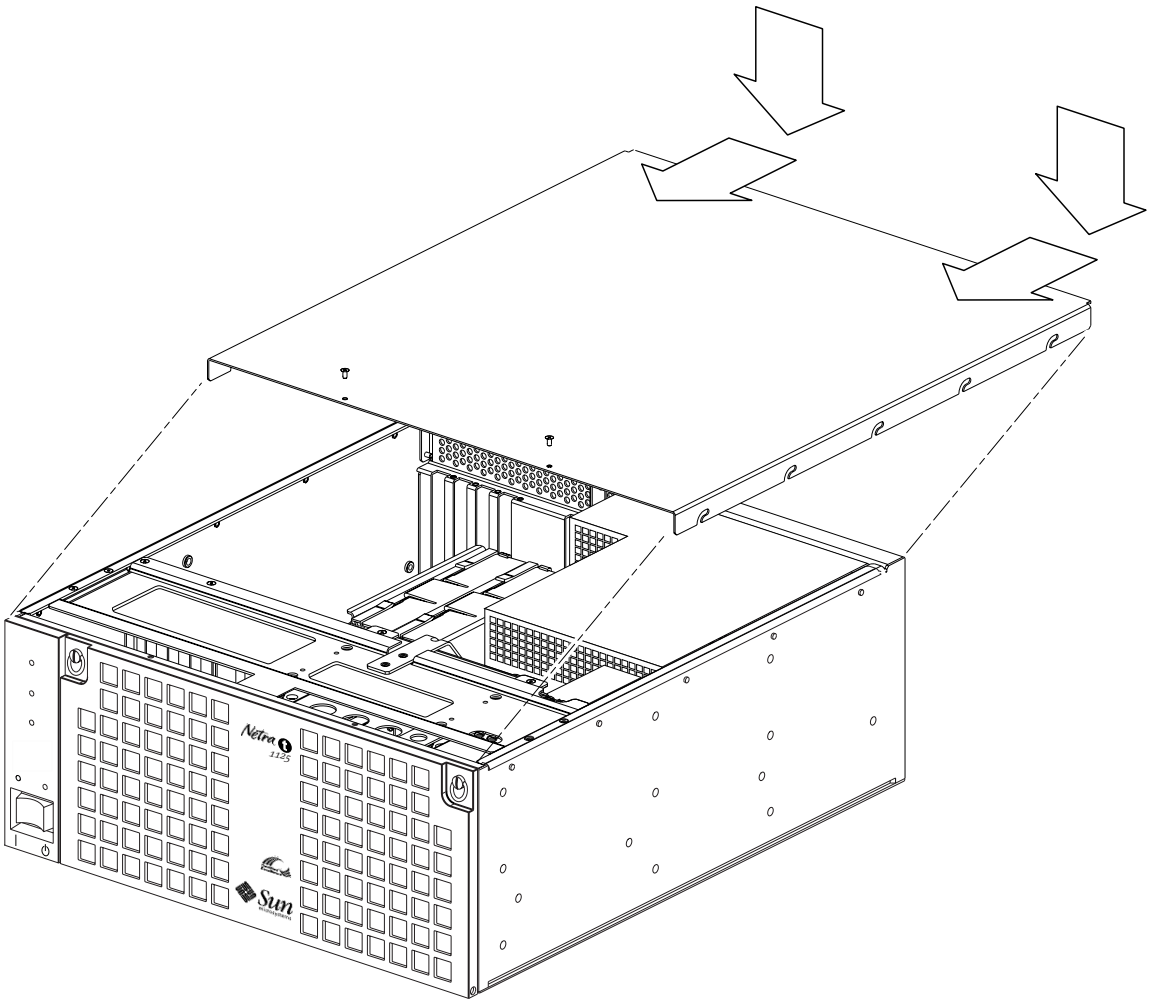


FIGURE 7-4 Replacing the Top Access Cover

CHAPTER 8

Power Subassemblies

This chapter contains procedures to remove and replace the power subassemblies of the Netra t 1120/1125 system unit enclosure.

8.1 Power Supply

8.1.1 To Remove the Power Supply

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

Caution – When removing the power supply, attach the copper end of the wrist strap to the system unit chassis, not to the power supply.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

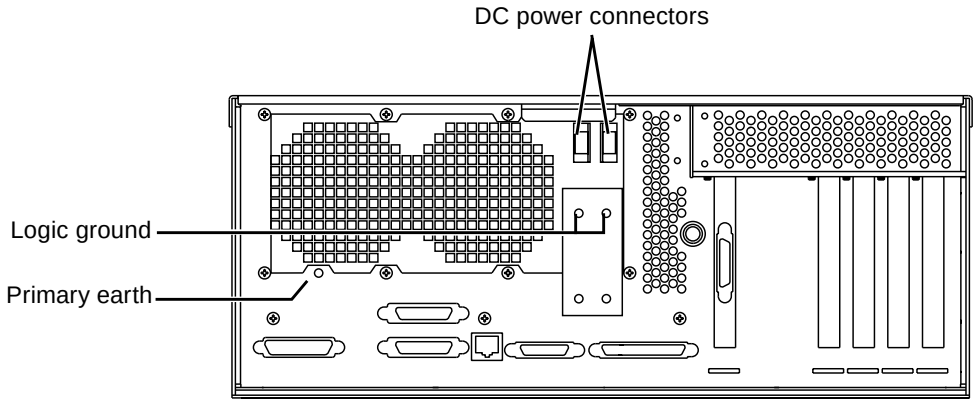


FIGURE 8-1 Netra t 1120 DC Power Connectors and Earth Points

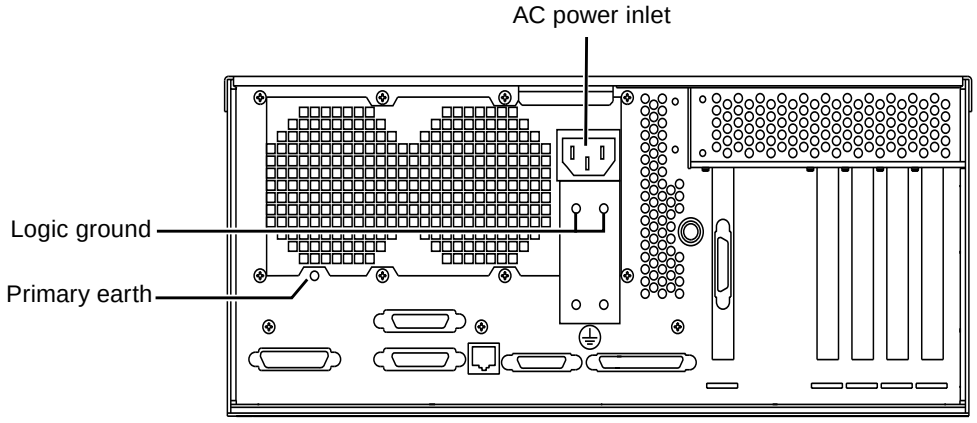


FIGURE 8-2 Netra t 1125 AC Power Inlet and Earth Points

4. **Using an 8mm wrench, remove the primary earth connection by removing the M5 nut and captive washer.**

5. **Using an 8mm wrench, remove the logic ground connection by removing the two M5 nuts and captive washers.**

6. **Using a No.2 Phillips-head screwdriver, loosen the eight external (see** FIGURE 8-3**) and two internal (see** FIGURE 8-4**) captive screws securing the power supply to the chassis.**

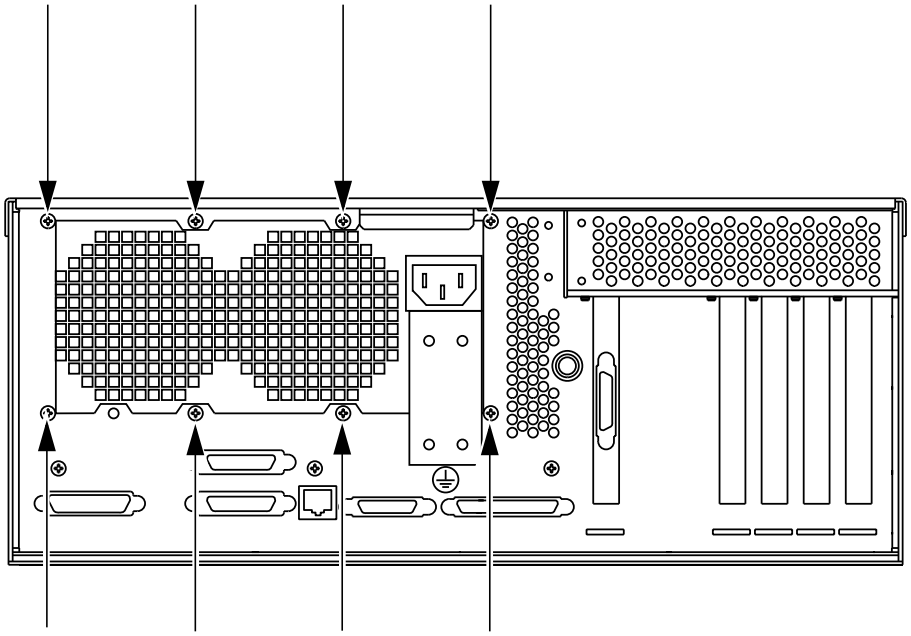


FIGURE 8-3 Removing the Power Supply (#1)

7. **Using a Phillips No. 2 screwdriver, remove the two captive screws securing the power supply bracket to the chassis front crossmember (see** FIGURE 8-4 **on page 8-4).**
8. **Push the power supply forwards slightly to clear the earth grounding stud.**
9. **Lift the power supply from the chassis until it is restrained by the power supply cables. Rest the power supply on the front crossmember of the enclosure.**
10. **Remove the cables from the clip retaining them to the processor mounting plate.**
11. **Disconnect the two cables from the alarms card. (To perform this it may be necessary to remove a PCI card from the chassis.)**
12. **Disconnect the power supply cables from the motherboard.**
13. **Disconnect the power supply cable from the removable drive assembly.**
14. **Disconnect the power supply cable from the hard disk drive assembly or assemblies.**

15. **Disconnect the power supply cable from the main fan unit.**

16. **Remove the power supply from the chassis.**

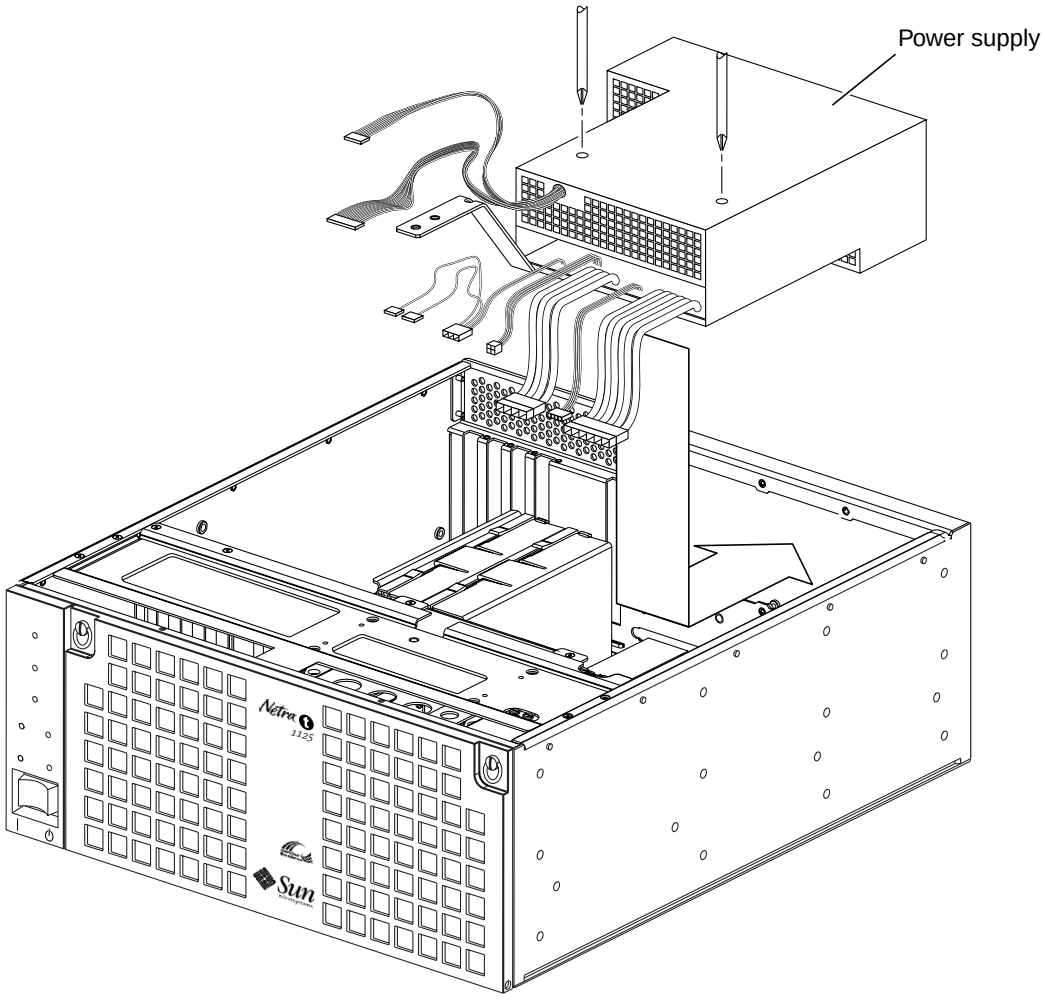


FIGURE 8-4 Removing the Power Supply (#2)

8.1.2 To Replace the Power Supply

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Position the power supply above the chassis. Rest it, upside-down (unlabeled side up), on the front crossmember of the enclosure.**
3. **Connect the power cable to the removeable media drive assembly (if fitted).**
4. **Connect the three main power supply cables to the motherboard.**
5. **Connect the power cable to the SCSI backplane assembly.**
6. **Connect the power cable to the main fan assembly.**
7. **Connect the cable connector to the alarms card.**
8. **Position the power supply toward the rear of the chassis until the power supply rear panel is flush with the chassis.**
9. **Using a No.2 Phillips-head screwdriver, tighten the eight captive screws securing the power supply to the rear of the chassis.**
10. **Using a No.2 Phillips-head screwdriver, tighten the two captive screws securing the power supply bracket to the chassis front crossmember.**
11. **Using a No.2 Phillips-head screwdriver, tighten the captive screw within the PSU to the chassis L-bracket.**
12. **Using an 8mm wrench, secure the primary earth connection by tightening the M5 nut and captive washer.**
13. **Using an 8mm wrench, secure the logic ground connection by tightening the two M5 nuts and captive washers.**
14. **Replace the top access cover.**

    See Section 7.3 “To Replace the Top Access Cover” on page 7-6.

15. **Reconnect the input power connector(s) and power on the system.**

    See Section 6.1 “To Power On the System” on page 6-2.

16. **Detach the wrist strap.**

8.2 ON / STBY Switch Assembly

8.2.1 To Remove the ON / STBY Switch Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system.**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Disconnect the ON/STBY switch connector from the back of the LED board.**

5. **Grasp both sides of the switch with the special tool supplied with the new switch, while pushing the switch towards the front of the system. Once free, the switch can be removed completely.**

6. **Remove the switch assembly from the chassis front. See** FIGURE 8-5 **on page 8-7.**

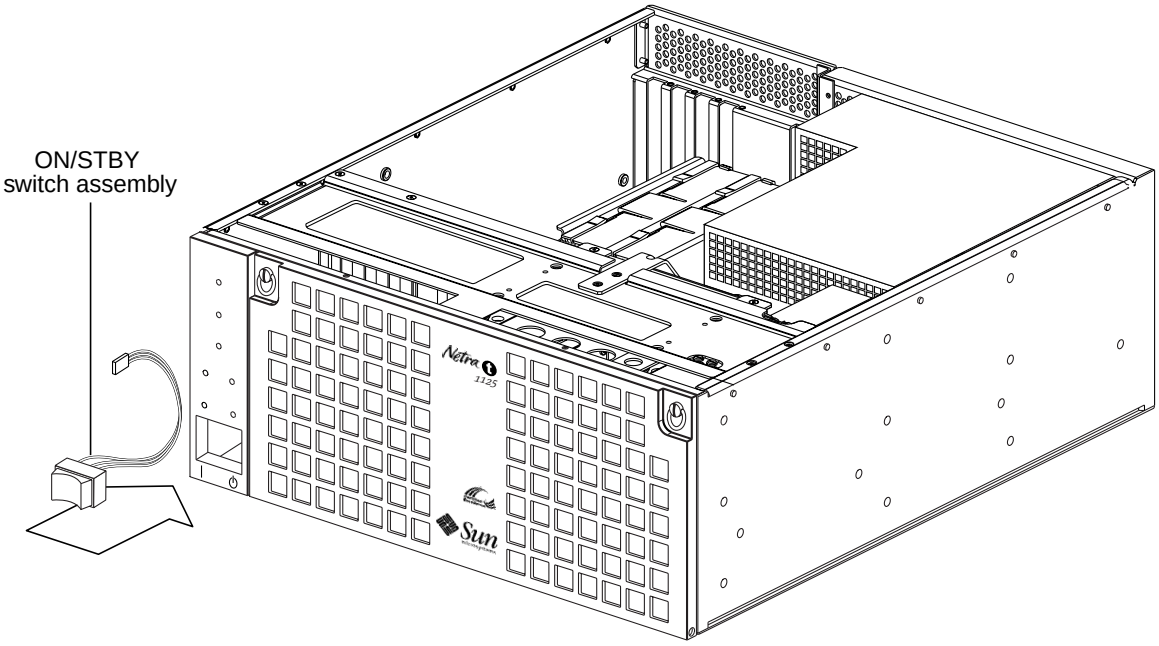


FIGURE 8-5 Removing and Replacing the ON/STBY Switch Assembly

8.2.2 To Replace the ON/STBY Switch Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Feed the switch assembly power connector through the chassis front.**
3. **Position the switch assembly into the chassis housing and snap it into place.**
4. **Connect the switch connector to the LED card.**
5. **Replace the top access cover.**

   See Section 7.3 “To Replace the Top Access Cover” on page 7-6.

6. **Detach the wrist strap.**

8.3 LED Card

8.3.1 To Remove the LED Card

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   SeeSection 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system.**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Remove the 10-way IDC cable from the alarms card.**

5. **Remove the 4-way molex connector from the rear of the LED card.**

6. **Use tool Part No. 250-1357-01 (provided with the replacement LED card) to manœuvre the LED card from the standoffs. See** FIGURE 8-6 **on page 8-10.**

7. **Place the LED card on an ESD mat.**

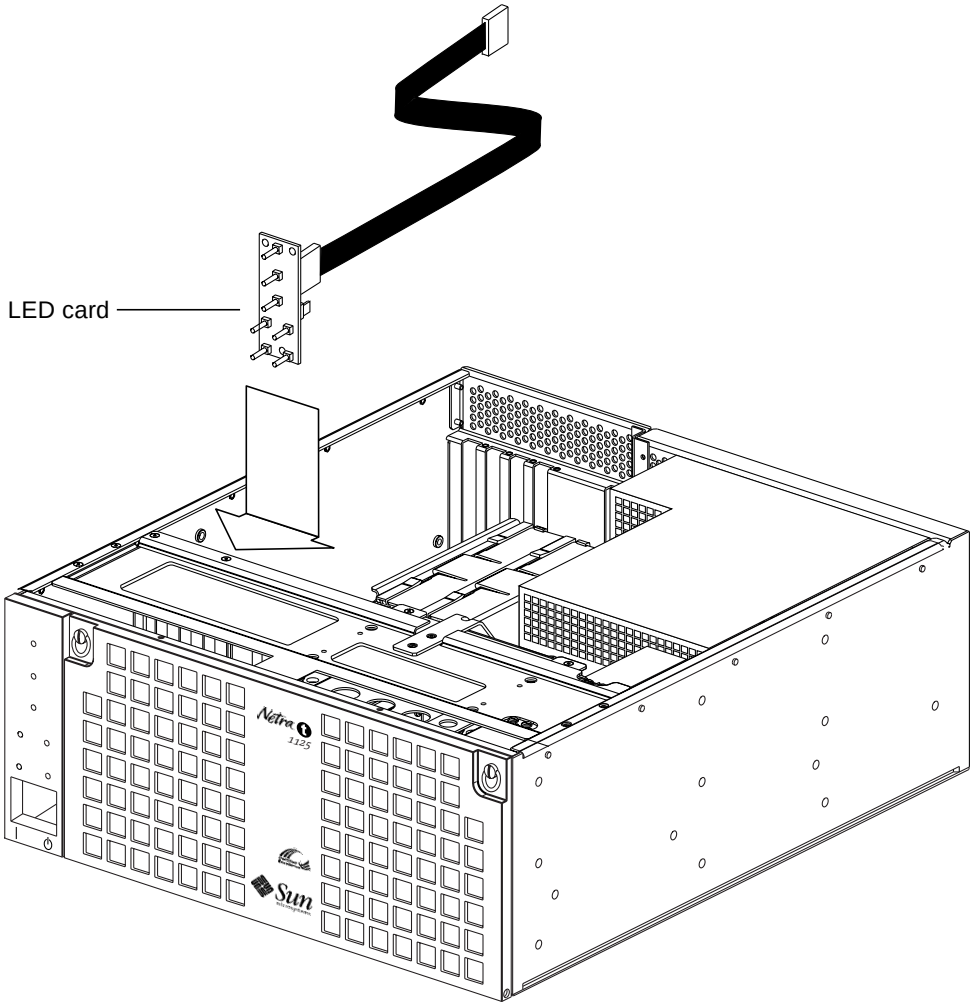


FIGURE 8-6 Removing and Replacing the LED Card

8.3.2 To Replace the LED Card

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Position the LED card in the chassis.**
3. **Carefully ensure all light pipes are aligned with the corresponding holes in the front panel.**
4. **Carefully push home the LED card until all the standoffs are fully engaged.**
5. **Reconnect the 10-way IDC cable to the alarms card.**
6. **Reconnect the 4-way power switch connector to the LED card.**
7. **Replace the top access cover.**

   See Section 7.3 “To Replace the Top Access Cover” on page 7-6.

8. **Detach the wrist strap.**

CHAPTER 9

Storage Devices

This chapter contains procedures to remove and replace the Netra t 1120/1125 system unit storage devices.

9.1 Hard Disk Drive

9.1.1 To Remove a Hard Disk Drive

See FIGURE 9-1 on page 9-3.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Open the front access cover.**
4. **Remove the front ESD screen, using a No.1 Phillips-head screwdriver to undo the two captive screws.**
5. **Push the handle latch to the right to open the drive handle.**
6. **Extend the drive handle to disconnect the drive from the system.**
7. **Holding the drive handle, remove the drive from the drive bay.**
8. **The hard disk drive rear connector is disconnected when the drive is ejected.**
9. **Place the drive on an ESD mat.**

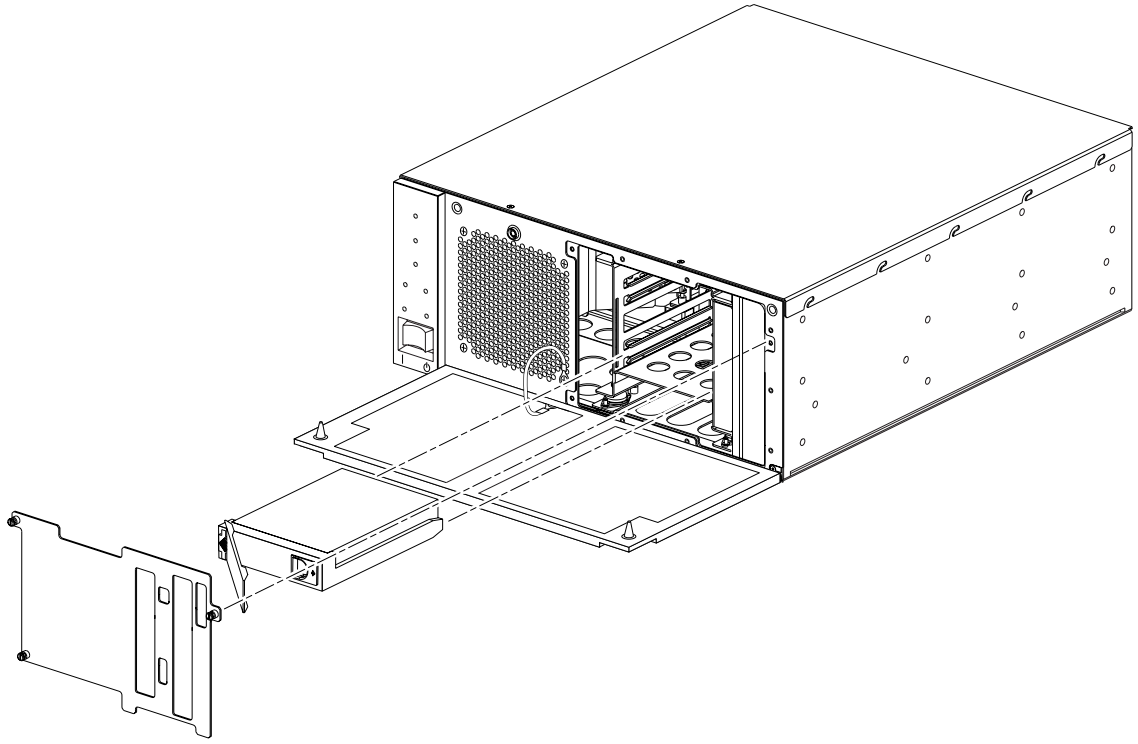


FIGURE 9-1 Removing and Replacing a Hard Disk Drive

9.1.2 To Install a Hard Disk Drive

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Holding the drive handle, insert the drive into the drive bay.**
4. **Push the front of the drive to connect it to the SCSI bus.**
5. **Close the drive handle to lock the drive into the system.**
6. **Replace the front ESD screen using a No.1 Phillips-head screwdriver.**
7. **Replace the front access cover.**
8. **Detach the wrist strap.**

9.2 Removable Media Drive

9.2.1 To Remove a Removable Media Drive

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Remove the ESD plate.**

   See Section 9.1.1 “To Remove a Hard Disk Drive” on page 9-2.

5. **Undo the four captive screws on top of the removable media drive assembly using a No.1 Phillips-head screwdriver.**

6. **Partially remove the CD-ROM/tape drive from the assembly.**

7. **Disconnect the SCSI and power connectors from the rear of the drive.**

8. **Remove the drive from the chassis and place it on an ESD mat.**

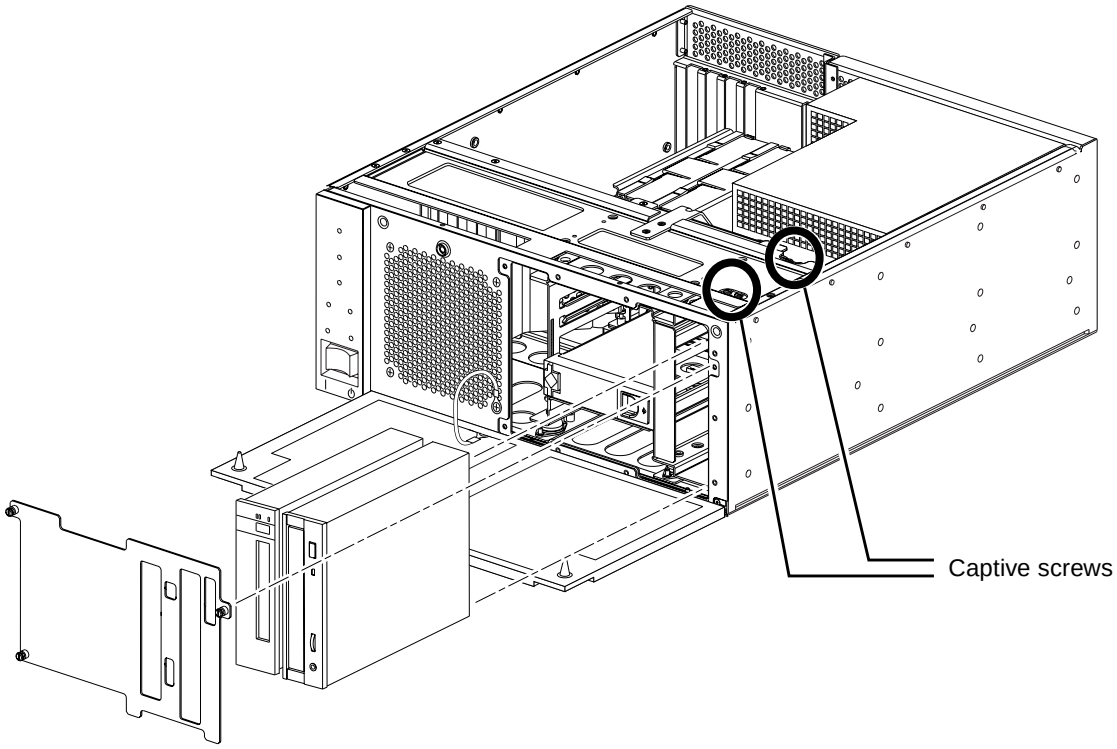


FIGURE 9-2 Removing and Replacing the CD-ROM or Tape Drive

9.2.2 To Install a Removable Media Drive

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Lower the front cover.**
5. **Remove the ESD plate.**
   See Section 9.1.1 “To Remove a Hard Disk Drive” on page 9-2.
6. **If necessary, remove the blanking plate.**
7. **Partially insert the drive with the release button at the top right hand side.**
8. **Connect the SCSI and power cables to the rear of the drive.**
9. **Push the drive fully into the drive assembly (**FIGURE 9-2 **on page 9-6).**
10. **Using a No.1 Phillips-head screwdriver, replace the four captive screws securing the drive to the drive assembly.**
11. **Replace the ESD plate.**
12. **Replace the top cover.**
    See Section 7.3 “To Replace the Top Access Cover” on page 7-6.
13. **Remove the wrist strap.**
14. **Replace the front cover.**

9.3 SCSI Backplane

9.3.1 To Remove the SCSI Backplane

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Remove the power supply.**

   See Section 8.1.1 “To Remove the Power Supply” on page 8-1.

5. **Remove the hard disk drive(s).**

   See Section 9.1.1 “To Remove a Hard Disk Drive” on page 9-2.

6. **Remove the CPU module(s).**

   See Section 10.1.1 “To Remove a CPU Module” on page 10-2.

7. **Remove the dual processor bracket.**

   See Section 10.1.3 “To Remove the Dual Processor Bracket” on page 10-4.

8. **Remove the SCSI connector from the removable media drive.**

9. **Using a No. 1 Phillips-head screwdriver, remove the four screws securing the SCSI backplane.**

   In order to perform this it may be necessary to remove some SIMMS; for information refer to Section 10.5.1 “To Remove a SIMM” on page 10-17.

10. **Disconnect the cable from the motherboard and feed the connector under the drive bay. Remove the SCSI backplane board from the chassis and place it on an ESD mat.**

9.3.2 To Replace the SCSI Backplane

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Remove the power supply.**

   See Section 8.1.1 “To Remove the Power Supply” on page 8-1.

5. **Feed the connector cable to the motherboard under the drive bay.**

6. **Using a No. 1 Phillips-head screwdriver, replace the four screws securing the SCSI backplane.**

7. **Replace the dual processor bracket.**

   See Section 10.1.4 “To Replace the Dual Processor Bracket” on page 10-6.

8. **Replace the CPU module(s).**

   See Section 10.1.2 “To Replace a CPU Module” on page 10-4.

9. **Replace any SIMMS which may have been removed.**

10. **Replace the power supply.**

    See Section 8.1.2 “To Replace the Power Supply” on page 8-5.

11. **Replace the top cover.**

    See Section 7.3 “To Replace the Top Access Cover” on page 7-6.

12. **Remove the wrist strap.**

13. **Replace the front cover.**

CHAPTER **10**

Motherboard and Component Replacement

This chapter contains removal and replacement procedures for the Netra t 1120/1125 motherboard and components of the motherboard.

10.1 CPU Modules

10.1.1 To Remove a CPU Module

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Using both thumbs, simultaneously lift the two levers on the CPU module upward and to the side.**

   See FIGURE 10-1 below.

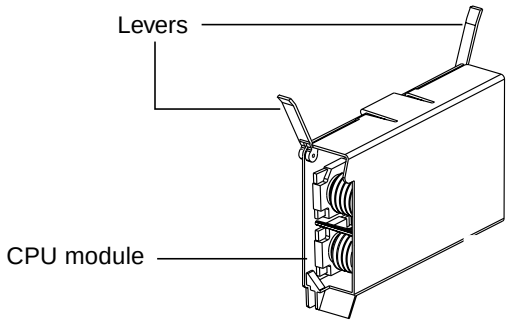


FIGURE 10-1 CPU Module Levers

5. **Using the two levers, lift the CPU module upwards until it clears the system chassis.**

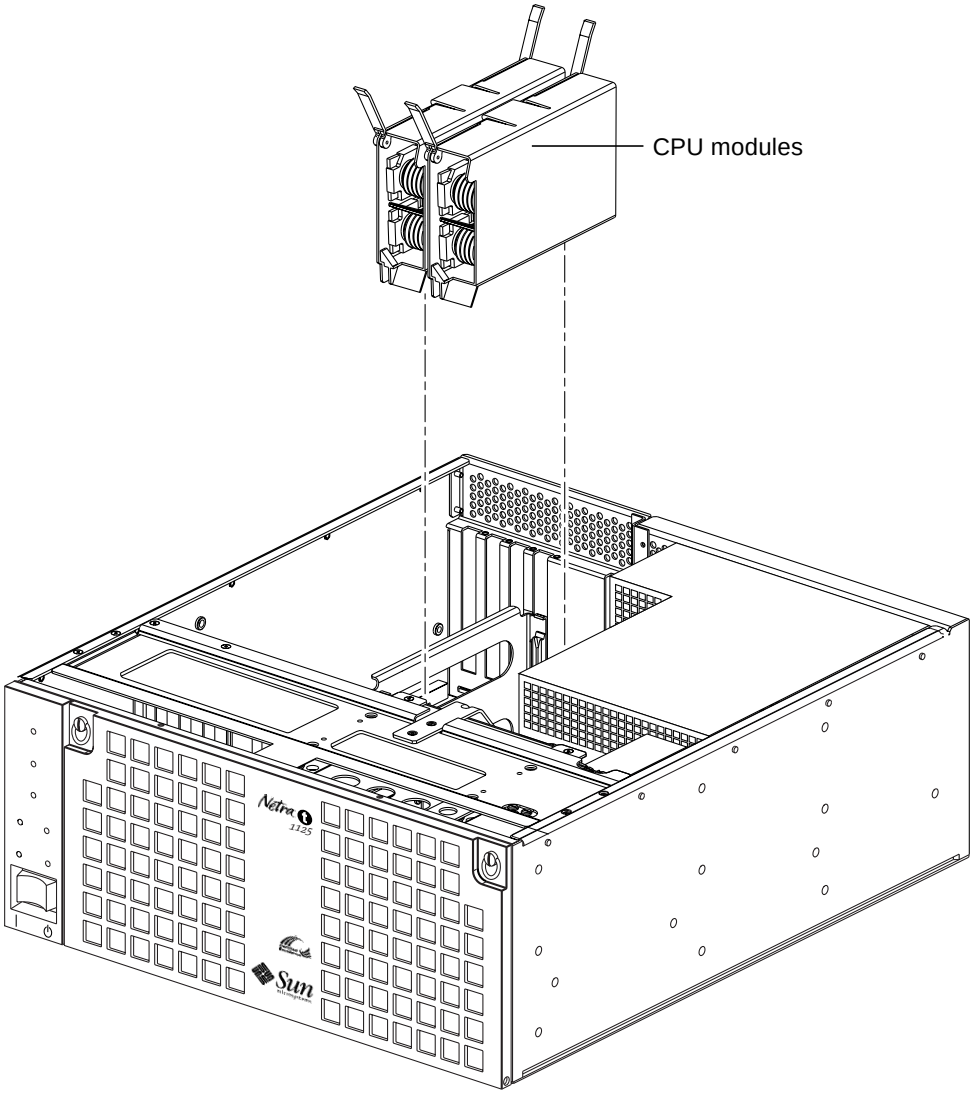


FIGURE 10-2 Removing and Replacing CPU Modules

6. **Place the CPU module on an ESD mat.**

10.1.2 To Replace a CPU Module

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the power cord.**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **On the antistatic mat, hold the CPU module in an upright position with the plastic surface facing you.**

4. **Move the levers on the CPU module to point straight upwards.**

5. **Lower the CPU module along the vertical plastic guides until the module touches the motherboard slot socket. Ensure connectors are aligned.**

   See (FIGURE 10-2 on page 10-3). With both hands, simultaneously turn and press the levers downward to the fully horizontal position.

6. **Firmly press the module downward into the socket until it is fully seated and the levers are fully locked.**

7. **Replace the top access cover.**

   See Section 7.3 “To Replace the Top Access Cover” on page 7-6.

8. **Detach the wrist strap.**

10.1.3 To Remove the Dual Processor Bracket

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the inputpower connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Remove the CPU module(s).**

   See Section 10.1.1 “To Remove a CPU Module” on page 10-2.

5. **Unplug the fan connectors from the motherboard and the power supply.**

6. **Using a No. 1 Phillips screwdriver, loosen the two captive screws securing the bracket to the motherboard (see** FIGURE 10-3**).**

   Tilt the bracket slightly to disengage the locating lugs from the keyholes in the motherboard and lift it off.

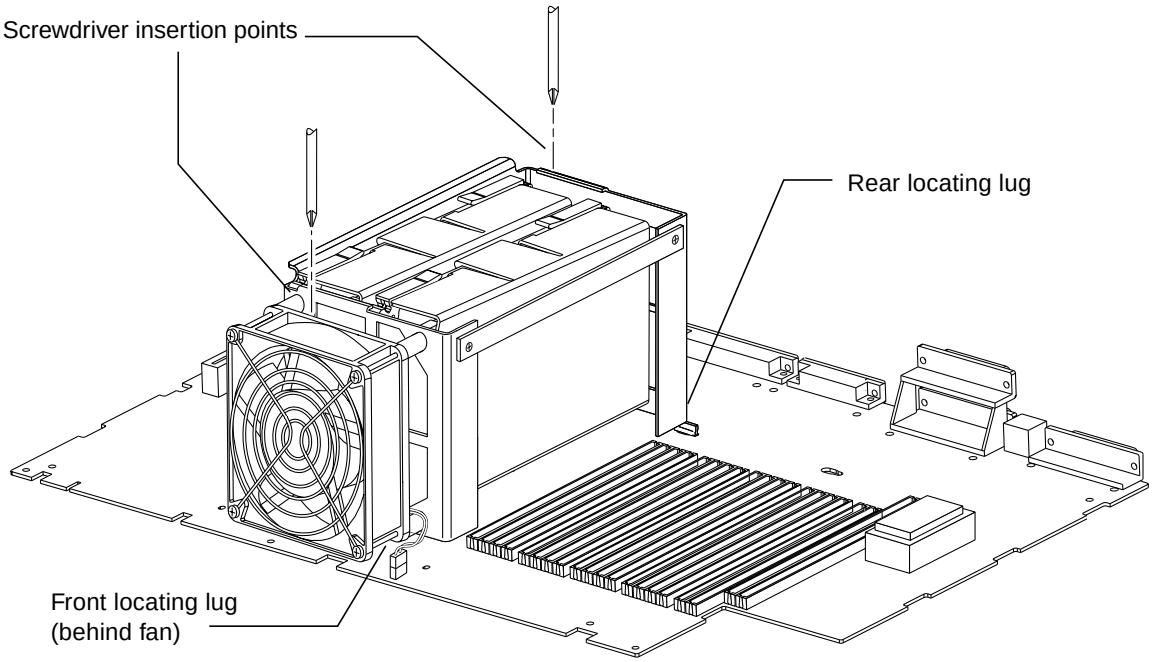


FIGURE 10-3 Removing the Dual Processor Bracket

10.1.4 To Replace the Dual Processor Bracket

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Carefully place the bracket on the motherboard so that the locating lugs engage in the keyholes and the captive screws align with the appropriate holes, then tighten the screws securely.**

3. **Plug in the connectors from the fan to the motherboard and the power supply.**

4. **Replace the CPU module(s).**

   See Section 10.1.2 “To Replace a CPU Module” on page 10-4.

5. **Replace the top access cover.**

   See Section 7.3 “To Replace the Top Access Cover” on page 7-6.

6. **Remove the wrist strap.**

10.2 System Fan Assembly

10.2.1 To Remove the System Fan Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Disconnect the fan assembly power cable from the power supply.**

5. **Using a No.2 Phillips-head screwdriver, undo the four screws and carefully remove the fan assembly from the chassis.**

   Note that the bottom right-hand screw secures the earth strap connection to the front cover.

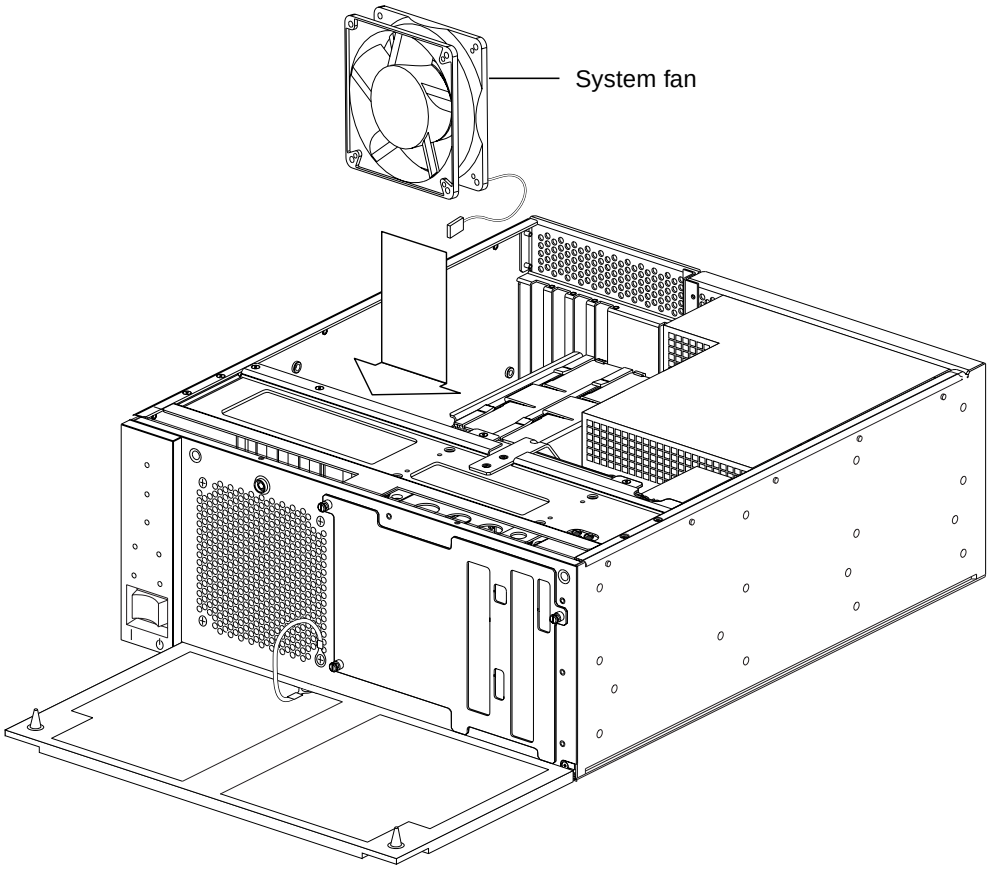


FIGURE 10-4 Removing and Replacing the System Fan Assembly

10.2.2 To Replace the System Fan Assembly

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Carefully position the fan assembly to the chassis and, using a No.2 Phillips-head screwdriver, secure with four screws.**

   Note that the bottom right-hand screw secures the earth strap connection to the front cover.

3. **Connect the fan assembly power cable to the power supply.**

4. **Replace the top access cover.**

   See Section 7.3 “To Replace the Top Access Cover” on page 7-6.

5. **Detach the wrist strap.**

6. **Power on the system.**

   See Section 6.1 “To Power On the System” on page 6-2.

10.3 NVRAM/TOD

Note – The NVRAM/TOD contains the system host identification (ID) and Ethernet address. If the same ID and Ethernet address are to be used on the replacement motherboard, remove the NVRAM/TOD from the motherboard and install the same NVRAM/TOD on the replacement motherboard after installation.

10.3.1 To Remove the NVRAM/TOD

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Remove the power supply from the system (without disconnecting the cables) and rest it on the enclosure.**

   See Section 8.1.1 “To Remove the Power Supply” on page 8-1.

5. **Locate the NVRAM/TOD and carrier on the motherboard.**

6. **Grasp the NVRAM/TOD carrier at each end and pull straight up.**

   Note – Gently rock the NVRAM/TOD from side to side as necessary.

7. **Place the NVRAM/TOD and carrier on an ESD mat.**

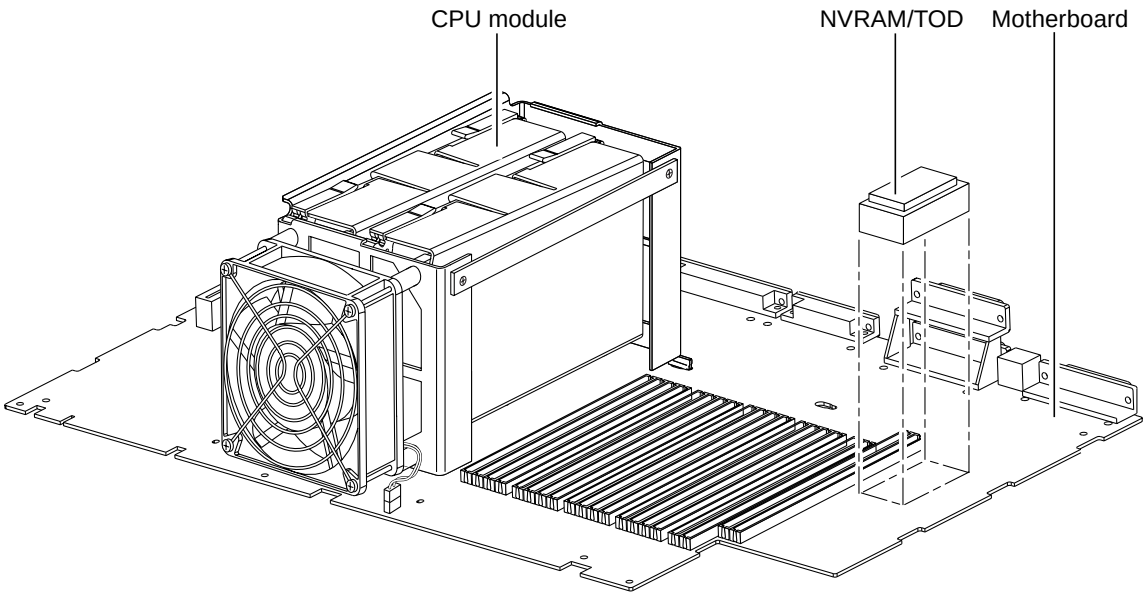


FIGURE 10-5 Removing and Replacing the NVRAM/TOD

10.3.2 To Replace a NVRAM/TOD

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Position the NVRAM/TOD and carrier on the motherboard.**
3. **Carefully insert the NVRAM/TOD and carrier into the socket.**

   Note – The carrier is keyed so the NVRAM/TOD can only be installed one way round.

4. **Push the NVRAM/TOD into the carrier until properly seated.**

5. **Replace the power supply.**

   See Section 8.1.2 “To Replace the Power Supply” on page 8-5.

6. **Replace the top access cover.**

   See Section 7.3 “To Replace the Top Access Cover” on page 7-6.

7. **Detach the wrist strap.**

10.4 PCI Card

10.4.1 To Remove a PCI Card

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Disconnect the cables from the PCI card to be removed.**

5. **Using a No.2 Phillips-head screwdriver, remove the screw securing the PCI card bracket tab to the system chassis.**

Caution – Avoid applying force to one end or one side of the board as this can damage the connector.

6. **Pull the PCI card straight upwards from the slot.**

7. **Place the PCI card on an ESD mat.**

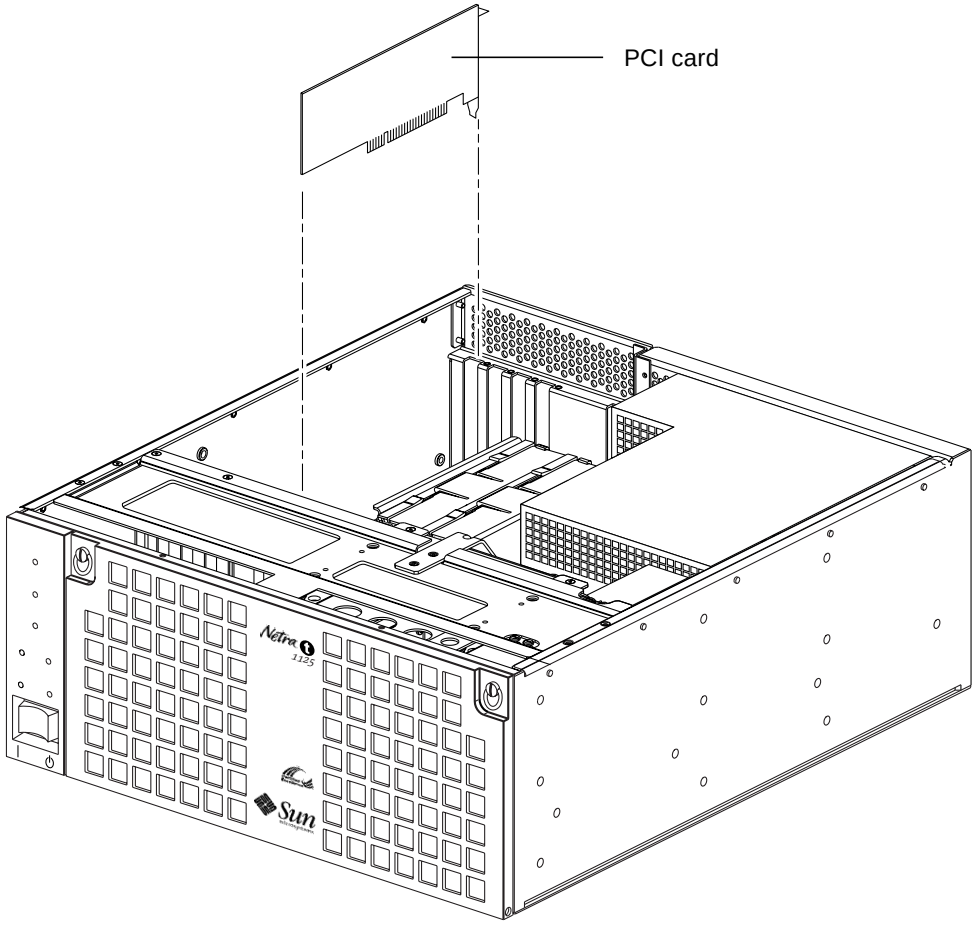


FIGURE 10-6 Removing and Replacing a PCI Card

10.4.2 To Replace a PCI Card

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

Note – Read the PCI card product guide for information about jumper or switch settings, slot requirements and required tools.

4. **Lower the PCI card so that it touches its associated slot on the motherboard.**
5. **From the two upper corners of the card, push the card straight downwards into the slot until it is fully seated.**
6. **Using a No.2 Phillips-headed screwdriver, insert and tighten the screw securing the card bracket tab to the system chassis.**
7. **Replace the top access cover.**

   See Section 7.3 “To Replace the Top Access Cover” on page 7-6.

8. **Connect the cables to the PCI card.**
9. **Power on the system.**

   See Section 6.1 “To Power On the System” on page 6-2.

10. **Detach the wrist strap.**

10.5 SIMMs

Caution – SIMMs consist of electronic components that are extremely sensitive to static electricity. Ordinary amounts of static electricity from clothing or work environment can destroy the SIMM.

Caution – When removing a SIMM, an identical replacement is required. The replacement SIMM must be inserted into the same socket as the removed SIMM.

Caution – Each SIMM bank must contain at least two SIMMs of equal density (for example, two 32Mbyte SIMMs) to function properly. Do not mix SIMM densities in any bank.

Note – The system unit *must* have at least two identical SIMMs installed in paired sockets of any SIMM bank. For best system performance, install four identical SIMMs. TABLE 10-1 identifies SIMM installation locations.

TABLE 10-1 SIMM Bank and Bank Quads

Bank	Bank Quad
0	U0701, U0702, U0703, and U0704
1	U0801, U0802, U0803, and U0804
2	U0901, U0902, U0903, and U0904
3	U1001, U1002, U1003, and U1004

10.5.1 To Remove a SIMM

Caution – Handle SIMMs only by the edges. Do not touch the SIMM components or metal parts. Always wear a grounding strap when handling a SIMM.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Remove the power supply but do not disconnect any restraining power supply cables.**

   See Section 8.1.1 “To Remove the Power Supply” on page 8-1.

5. **Rest the power supply on the side of the system enclosure.**

6. **Locate the SIMM to be removed.**

7. **Push the lever away from the SIMM (see** FIGURE 10-7 **on page 10-18) to be removed.**

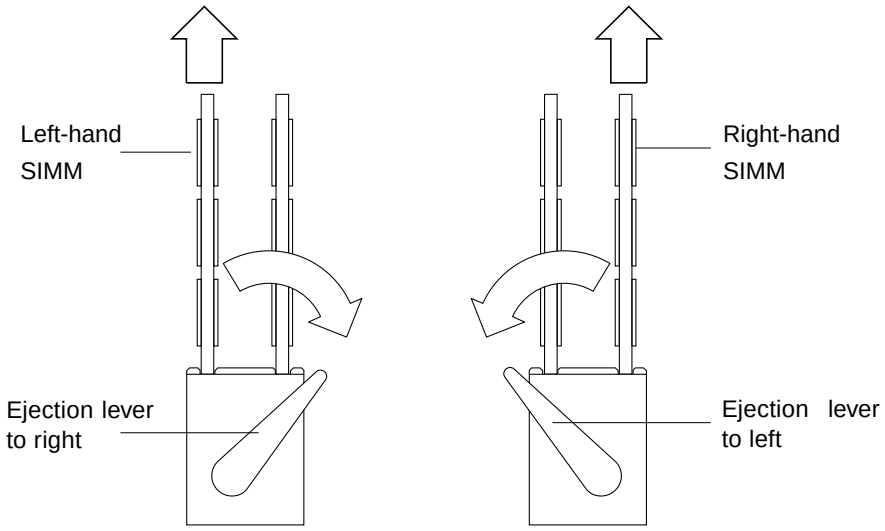


FIGURE 10-7 SIMM Ejection Lever

8. **Remove the SIMM from the socket (see** FIGURE 10-8 **on page 10-19).**
9. **Place the SIMM on an ESD mat.**

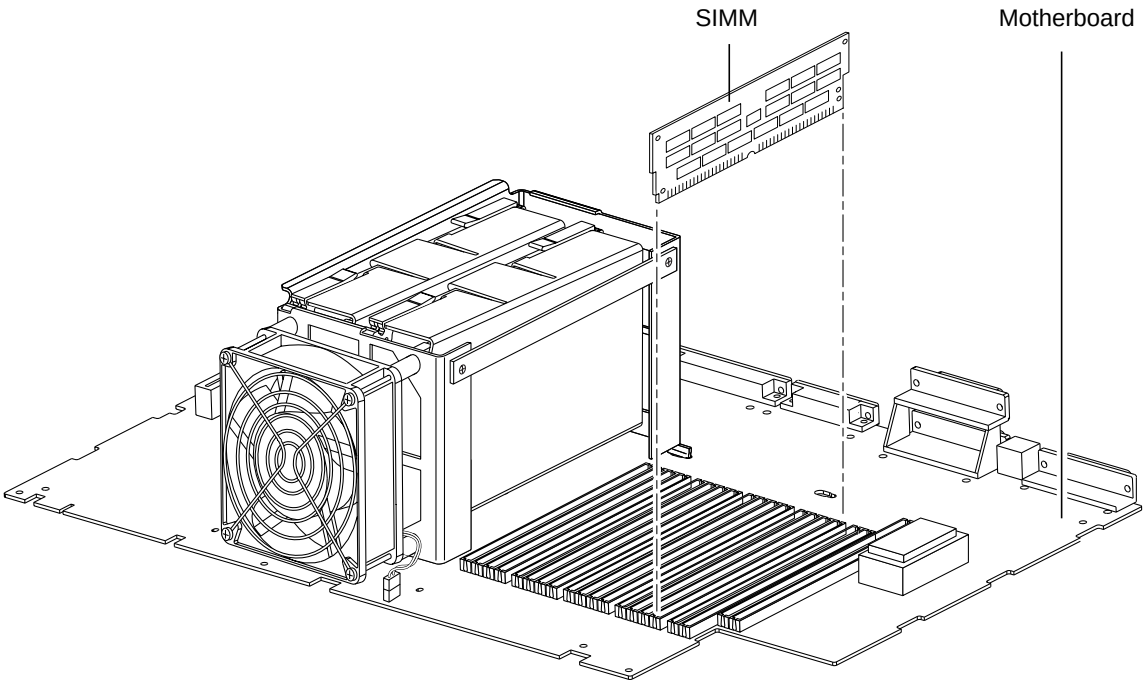


FIGURE 10-8 Removing and Replacing a SIMM

10.5.2 To Replace a SIMM

Caution – SIMMs are made of electronic components that are extremely sensitive to static electricity. Ordinary amounts of static electricity from clothing or work environment can destroy the SIMM.

Caution – Do not remove any SIMM from the antistatic container until ready to install it on the motherboard. Handle SIMMs only by their edges. Do not touch SIMM components or metal parts. Always wear an antistatic wrist strap when handling SIMMs.

Caution – Each SIMM bank must contain two SIMMs of equal density (for example, two 32Mbyte SIMMs) to function properly. Do not mix SIMM density in any bank.

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Locate the appropriate SIMM slot(s) on the motherboard.**

Note – The system unit *must* have at least two identical SIMMs installed in paired sockets of any SIMM bank. For best system performance, install four identical SIMMs. TABLE 10-1 identifies SIMM installation locations.

Caution – Hold SIMMs only by the edges.

3. **Remove the SIMM from the antistatic container.**
4. **Position the SIMM in the socket, ensuring that the notch is on the same side as the lever.**
5. **Using your thumbs, press firmly on the top of the SIMM until it is properly seated.**

Note – Proper SIMM seating is verified by a clicking sound. Ensure the SIMM is properly seated.

6. **Replace the power supply.**

   See Section 8.1.2 “To Replace the Power Supply” on page 8-5.

7. **Replace the top access cover.**

   See Section 7.3 “To Replace the Top Access Cover” on page 7-6.

8. **Power on the system.**

   See Section 6.1 “To Power On the System” on page 6-2.

9. **Detach the wrist strap.**

10.6 Alarms Card

10.6.1 To Remove the Alarms Card

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Remove the connector from the alarms card.**

5. **Using a No.2 Phillips-head screwdriver, remove the screw securing the alarms card bracket tab to the system chassis.**

Caution – Avoid damaging the connector. Apply equal force to both ends or sides of the board.

6. **At the two upper corners of the alarms card, pull the card straight upward from the slot. See** FIGURE 10-9 **on page 10-22.**

7. **Remove the alarms card.**

8. **Disconnect the cables from the alarms card.**

9. **Place the alarms card on an ESD mat.**

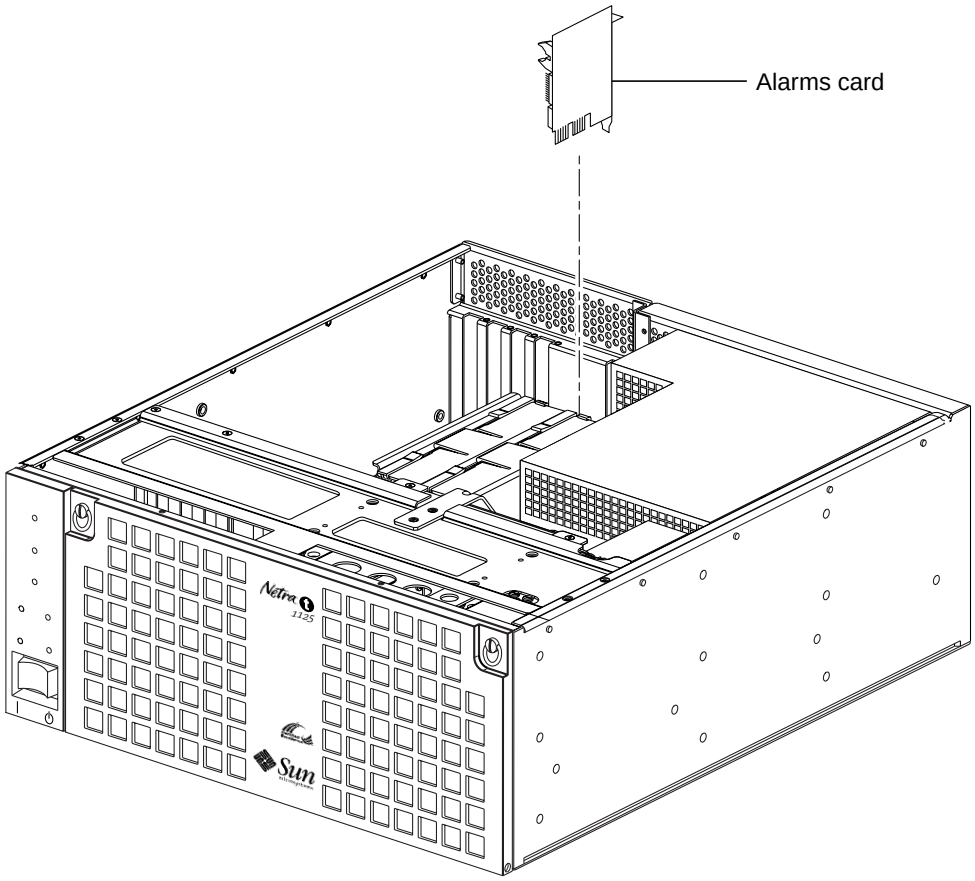


FIGURE 10-9 Removing and Replacing the Alarms Card

10.6.2 To Replace the Alarms Card

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Position the alarms card into the chassis.**
3. **Lower the alarms card so that it touches the appropriate slot on the motherboard.**
4. **At the two upper corners of the card, push the card straight downwards into the slot until it is fully seated.**
5. **Using a No.2 Phillips-head screwdriver, replace the screw securing the alarms card to the system chassis.**
6. **Reconnect the cables to the alarms card.**
7. **Replace the top access cover.**

   See Section 7.3 “To Replace the Top Access Cover” on page 7-6.

8. **Power on the system.**

   See Section 6.1 “To Power On the System” on page 6-2.

9. **Detach the wrist strap.**

10.7 Motherboard

Caution – Use an ESD mat when working with the motherboard. An ESD mat contains the cushioning needed to protect the underside components, to prevent motherboard flexing, and to provide antistatic protection.

Note – If the motherboard is being replaced, remove all SIMMs, PCI card(s), alarms card, and CPU module prior to removing the motherboard. Note the chassis slot location for each SIMM and PCI card prior to removal.

Note – The NVRAM/TOD contains the system host identification (ID) and Ethernet address. If the same ID and Ethernet address are to be used on the replacement motherboard, remove the NVRAM/TOD from the motherboard and install the same NVRAM/TOD on the replacement motherboard after installation.

10.7.1 To Remove the Motherboard

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach the wrist strap to the rear of the chassis.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1.

2. **Power off the system and remove the input power connector(s).**

   See Section 6.2 “To Power Off the System” on page 6-3.

3. **Remove the top access cover.**

   See Section 7.2 “To Remove the Top Access Cover” on page 7-4.

4. **Remove the power supply.**

   See Section 8.1.1 “To Remove the Power Supply” on page 8-1.

5. **Depopulate the motherboard by removing the following:**

   a. **CPU module(s).**

      See Section 10.1.1 “To Remove a CPU Module” on page 10-2.

   b. **Dual processor bracket.**

      See Section 10.1.3 “To Remove the Dual Processor Bracket” on page 10-4.

   c. **NVRAM/TOD with carrier.**

      See Section 10.3.1 “To Remove the NVRAM/TOD” on page 10-10.

   d. **Alarms card.**

      See Section 10.6.1 “To Remove the Alarms Card” on page 10-21.

   e. **PCI card(s).**

      See Section 10.4.1 “To Remove a PCI Card” on page 10-13.

   f. **SIMMs.**

      See Section 10.5.1 “To Remove a SIMM” on page 10-17.

6. **Disconnect the SCSI cable.**

7. **Disconnect the external cables.**

8. **Using a No.2 Phillips-head screwdriver, undo the three captive screws securing the motherboard to the rear chassis panel.**

   .

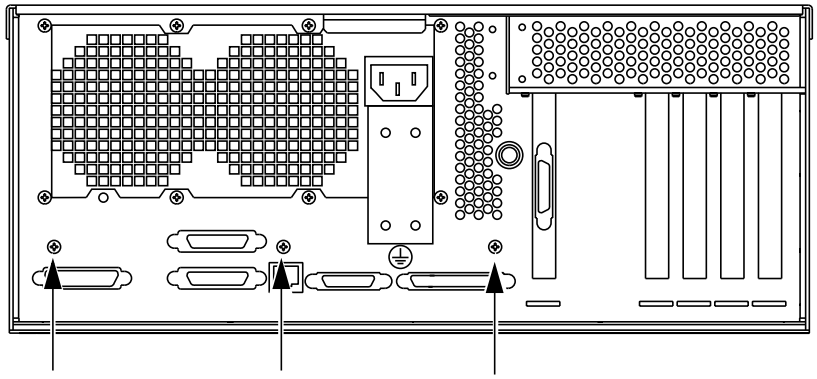


FIGURE 10-10 Removing and Replacing the Motherboard (#1)

9. **Remove the motherboard by sliding it towards the front of the chassis slightly, then raising the left-hand-side (viewed from the front of system).**

Caution – Handle the motherboard by the handle, back panel, or the edges only.

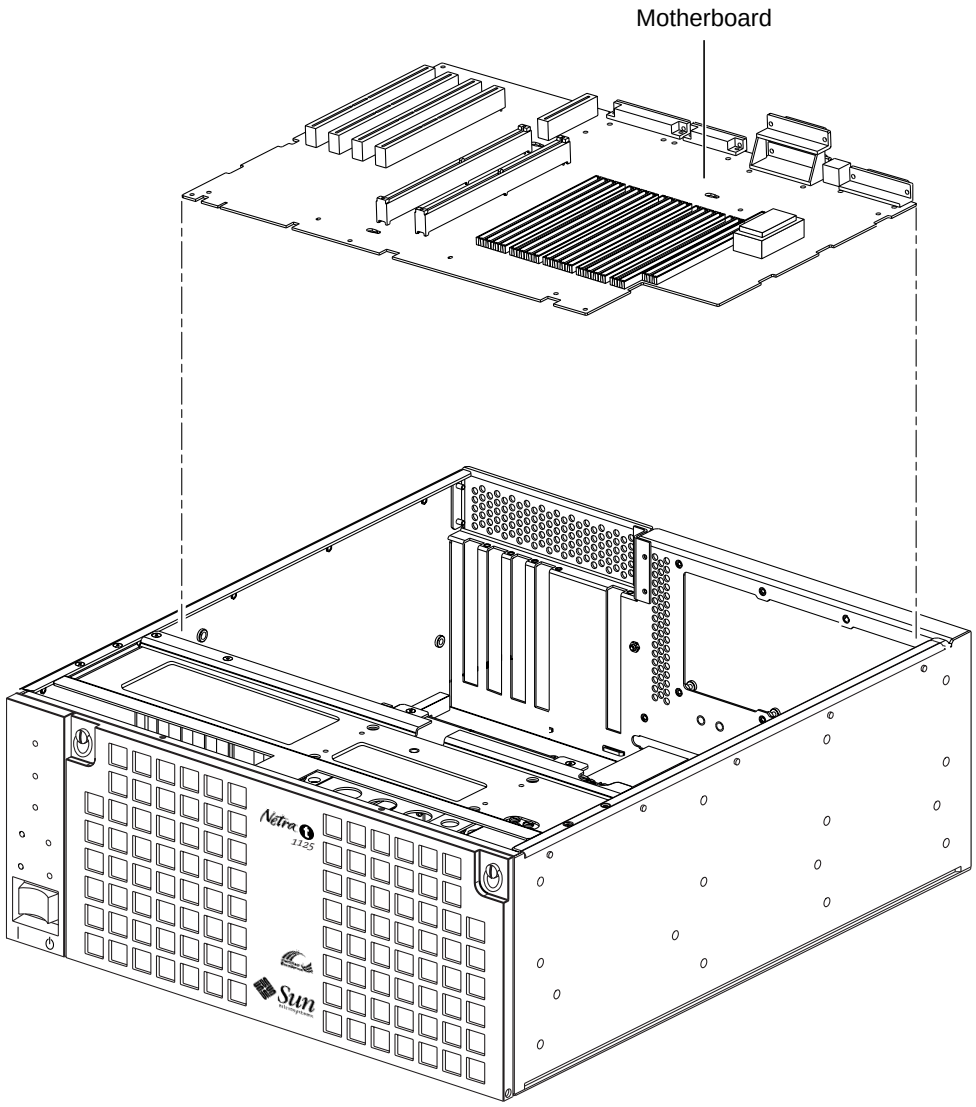


FIGURE 10-11 Removing and Replacing the Motherboard (#2)

10. Place the motherboard on an ESD mat.

10.7.2 To Replace the Motherboard

Caution – Use proper ESD grounding techniques when handling components. Wear an antistatic wrist strap and use an ESD-protected mat. Store ESD-sensitive components in antistatic bags before placing them on any surface.

1. **Attach a wrist strap to the rear of the chassis.**

   See Section 7.1 “To Attach the Wrist Strap” on page 7-1

Caution – Handle the motherboard by the handle, back panel, or the edges only.

2. **Grasp the handle and the rear connector panel and slide the motherboard into the chassis (See** FIGURE 10-11 **on page 10-26).**
3. **Using long-nose pliers, set the motherboard serial port jumpers J2604 and J2605 (**TABLE 10-2 **below and** FIGURE 10-12 **on page 10-29).**

TABLE 10-2 Serial Port Jumper Settings

Port	Jumper	Pins 1 + 2 Select	Pins 2 + 3 Select	Default Shunt on Pins
ttya	J2604	RS232	RS423	2 + 3
ttyb	J2605	RS232	RS423	2 + 3

Note – Jumpers J2604 and J2605 can be set to either RS423 or RS232 serial interface. The jumpers are preset for RS423. RS232 is required for digital telecommunication within the European Community.

4. **Using a No.2 Phillips-head screwdriver, tighten the three captive screws that secure the motherboard to the rear of the chassis panel (see** FIGURE 10-10 **on page 10-25) starting with the centre screw.**
5. **Connect the external cables.**
6. **Populate the motherboard by replacing the following:**

   a. **SIMMs.**
   See Section 10.5.2 “To Replace a SIMM” on page 10-19.

   b. **PCI card(s).**
   See Section 10.4.2 “To Replace a PCI Card” on page 10-15.

c. **Alarms card.**

See Section 10.6.2 “To Replace the Alarms Card” on page 10-23.

d. **NVRAM/TOD with carrier.**

See Section 10.3.2 “To Replace a NVRAM/TOD” on page 10-11.

e. **Dual processor bracket.**

See Section 10.1.4 “To Replace the Dual Processor Bracket” on page 10-6.

f. **CPU module(s).**

See Section 10.1.2 “To Replace a CPU Module” on page 10-4.

7. **Replace the power supply.**

See Section 8.1.2 “To Replace the Power Supply” on page 8-5.

8. **Replace the top access cover.**

See Section 7.3 “To Replace the Top Access Cover” on page 7-6.

9. **Power on the system.**

See Section 6.1 “To Power On the System” on page 6-2.

10. **Detach the wrist strap.**

11. **Reset the `#power-cycles` NVRAM variable to zero as follows:**

a. **Set system power to on.**

See Section 6.1 “To Power On the System” on page 6-2.

b. **Send a Break command after the system banner appears on the monitor.**

c. **At the `ok` prompt, type:**

```
ok setenv #power-cycles 0
```

d. **Verify that the `#power-cycles` NVRAM variable increments each time the system is power cycled.**

Note – The Solaris operating environment Power Management software uses the `#power-cycles` NVRAM variable to control the frequency of automatic system shutdown, if it is enabled.

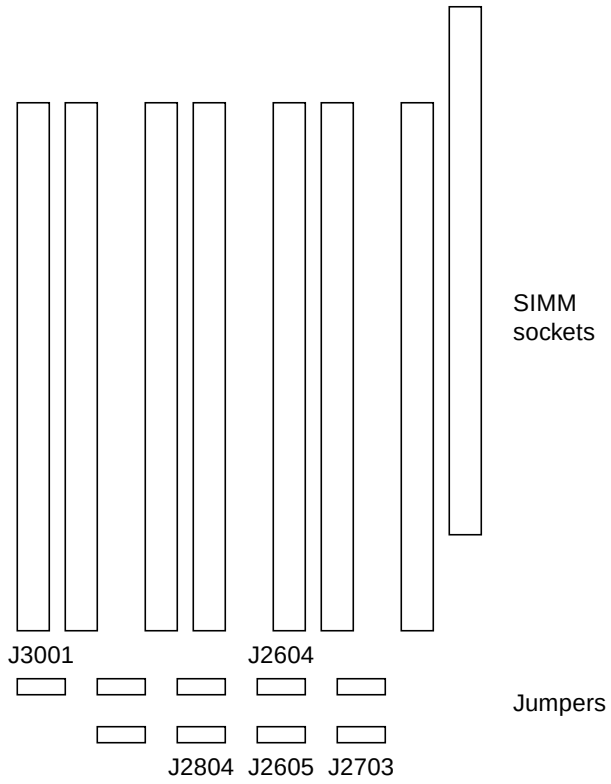


FIGURE 10-12 Location of the Motherboard Serial Port Jumpers

Note – Motherboard jumpers are identified with location numbers. Jumper pins are located immediately adjacent to the location number. Pin 1 is marked with an asterisk in any of the positions shown (FIGURE 10-13). Ensure that the serial port jumpers are set correctly.

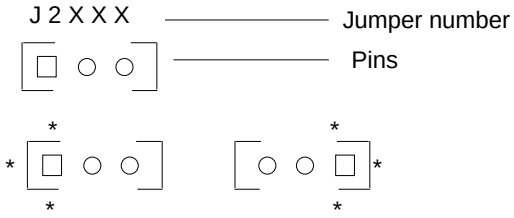


FIGURE 10-13 Identifying Jumper Pins

APPENDIX **A**

Illustrated Parts List

This chapter lists the authorized replaceable parts for the Netra t 1120/1125 system unit. FIGURE A-1 on page A-2 illustrates an exploded view of the system unit. TABLE A-1 on page A-3 lists the replaceable components. A brief description of each listed component is also provided.

The part numbers listed in TABLE A-1 are correct as of the service manual publication date but are subject to change without notice. Numerical references illustrated in FIGURE A-1 correlate to the numerical references listed in TABLE A-1. Consult your authorized Sun sales representative or service provider to confirm a part number prior to ordering a replacement part.

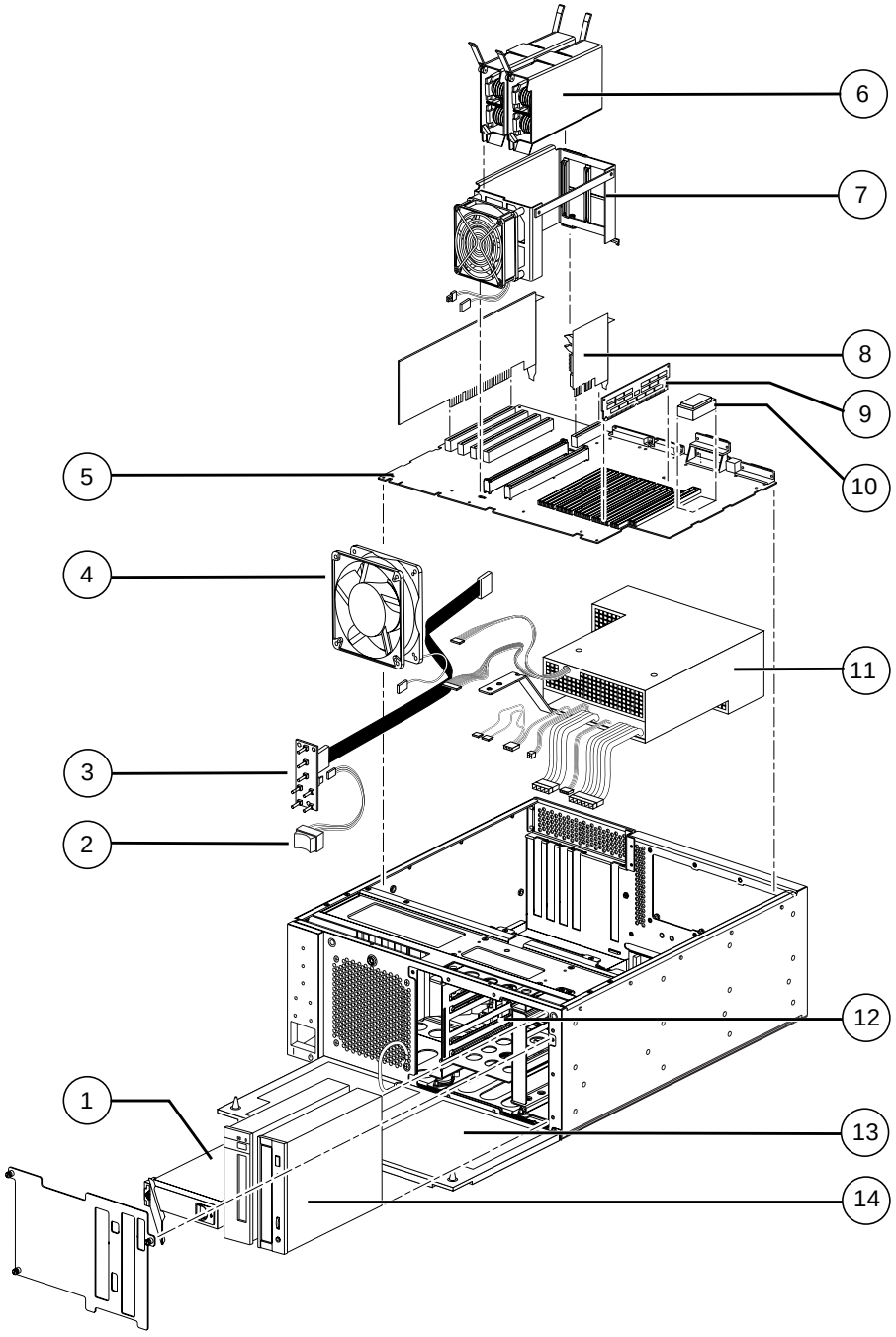


FIGURE A-1 System Exploded View

TABLE A-1 Replaceable Components

Numerical Reference	Component	Part Number	Description
1	4.2Gbyte SCSI assembly	540-2938	Hard disk drive
1	9.1Gbyte SCSI assembly	540-2951	Hard disk drive
1	18Gbyte SCSI assembly	540-3739	Hard disk drive
2	ON/STBY power switch	530-2514	On/Standby power switch
3	LED card	501-4670	LED card
4	Main fan assembly	540-3514	Main fan
5	Motherboard	501-3139	System board
6	CPU module	501-4849	300MHz, 2Mbyte external cache
7	Dual processor bracket	540-3809	Processor mounting bracket and fan
8	Alarms module	501-4669	Alarms applications
9	32Mbyte SIMM	501-2622	60ns, 32Mbyte DSIMM
9	64Mbyte SIMM	501-2480	60ns, 64Mbyte DSIMM
9	128Mbyte SIMM	501-3136	60ns, 128Mbyte DSIMM
10	NVRAM/TOD	525-1430	Time of day, 48T59, with carrier
11	Power supply	300-1406	Power supply
12	SCSI Backplane	530-6924	SCSI Backplane and QCD
13	Air Filter	250-1392	Air Filters (Qty 10)
14	CD-ROM drive	370-2817	12x CD-ROM drive, 1.6 inches
14	2.5Gbyte QIC tape drive 4.0Gbyte tape drive	370-2018 370-5280	2.5Gbyte QIC tape drive, light gray 4.0Gbyte SLR-5 tape drive, dark gray
14	4mm tape drive	370-2176	4Gbyte/8Gbyte, 4mm tape drive, DDS-2, light gray

TABLE A-1 Replaceable Components *(Continued)*

Numerical Reference	Component	Part Number	Description
14	4mm tape drive	370-2376	12Gbyte/24Gbyte, 4mm tape drive, DDS-3, dark gray
14	8mm tape drive	370-2822	14Gbyte, 8mm tape drive, dark gray
Not illustrated	Peripheral cable	530-2345	Peripheral cable
Not illustrated	Filler panel	330-2187	CD-ROM drive filler panel
Not illustrated	SCSI cable	530-2384	68-pin external SCSI cable (2m)
Not illustrated	SCSI cable	530-2383	68-pin external SCSI cable (0.8m)

APPENDIX **B**

Product Specifications

This appendix provides product specifications for the Netra t 1120/1125 system unit and is divided into three parts:

- Physical specifications
- Electrical specifications
- Environmental requirements.

B.1 Physical Specifications

TABLE B-1 Physical Specifications

Specification	Imperial	Metric
Width	17.13in.	431.8mm
Height	7.00in. (4U)	177mm
Depth	19.53in.	496.1mm
Weight (approximate, system unit equipped with four SIMMs, two hard disk drives and one CD-ROM drive)	51lb	23kg

B.2 Electrical Specifications

B.2.1 XL

TABLE B-2 Netra t 1120 Electrical Specifications

Parameter	Value
DC input	–48Vdc and –60Vdc nominal
DC output	350W (maximum)
Output 1	+3.3Vdc, 50A
Output 2	+5.0Vdc, 35A
Output 3	+12.0Vdc, 6.0A
Output 4	–12.0Vdc, 1.0A
Output 5	–Prog 2.5V 28A

B.2.2 an XL

TABLE B-3 Netra t 1125 Electrical Specifications

Parameter	Value
DC input	110 and 240Vac nominal 90 to 264Vac, 47 to 63Hz
DC output	325W (maximum)

B.3 Environmental Requirements

TABLE B-4 Environmental Requirements

Environmental	Operating	Non-operating
Temperature	5° to 40°C	–40° to 70°C
Short term temperature (short term is defined as a maximum of 96 consecutive hours.)	–5° to 55°C (at a maximum of 1800m) Error-free operation of the tape streamer is from 0°C to 40°C.	
Humidity	5 to 85% (non-condensing)[1] (5 to 90% for a maximum 96 hours.)	10 to 95% non-condensing at 104°F (40°C)[1]
Elevation	–300 to +3000m	–300 to +12000m
Acoustic Noise	Less than 60dBA at a distance of 600mm and a height of 1500mm, measured at 25°C.	

1. Subject to a maximum absolute humidity of 0.024kg of water / kg of dry air.

APPENDIX **C**

Signal Descriptions

This appendix provides signal descriptions for the Netra t 1120/1125 system unit motherboard connectors. Connector pin assignments and signal descriptions are provided, as well as an illustration of each connector.

C.1 Connector Layout

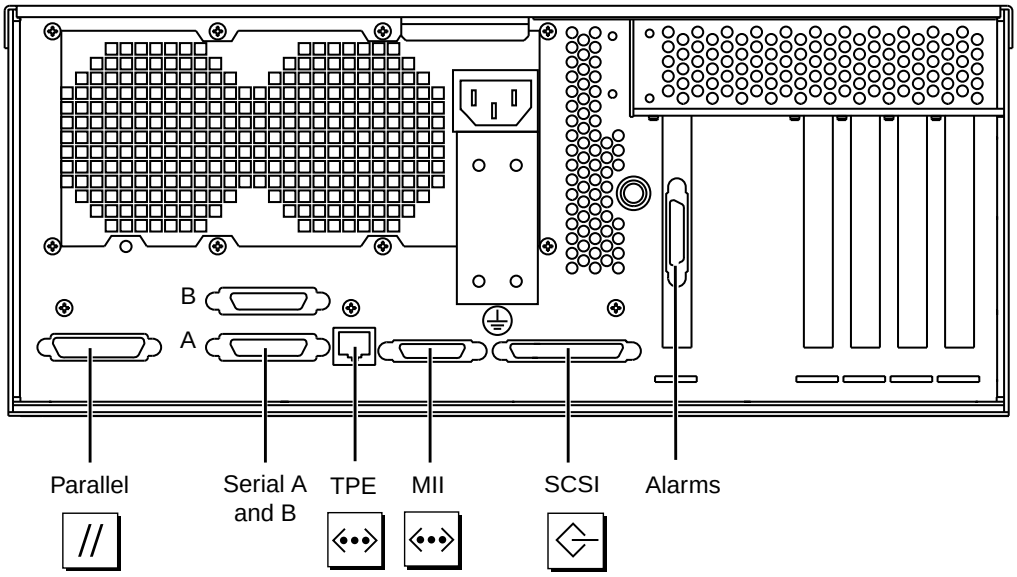


FIGURE C-1 System Unit Rear View

C.2 Serial Ports A and B

The serial port A and B connectors are DB-25 connectors located on the system board back panel. FIGURE C-2 illustrates the serial ports A and B connector configuration, and TABLE C-1 lists the connector pin assignments.

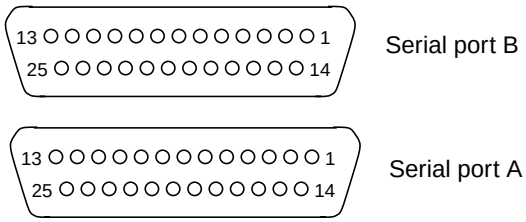


FIGURE C-2 Serial Ports A and B Connector Pin Configuration

TABLE C-1 Serial Port Pinouts

Pin	Mnemonic	Signal Name	Description
1		Not connected	None
2	TxD	Transmit Data	Used by the data terminal equipment (DTE) to transmit data to the data circuit terminating equipment (DCE). Except when control data is being sent, RTS, CTS, SYNC and DCD must be ON for this line to be active.
3	RxD	Receive Data	Used by the DCE in response to received data from the DTE.
4	RTS	Ready To Send	Used by the DTE to condition the DCE for data transmission. The transition to ON directs the DCE to go into transmit mode. The transition to OFF directs the DCE to complete the transmission.
5	CTS	Clear To Send	Used by the DCE to indicate if it is ready to receive data from the DTE. When CTS, DSR, RTS and DTR are ON, the DCE is ready to transmit data received from the DTE across the communications channel. When only CTS is ON, the DCE is ready to accept dialing or control signals only. When CTS is OFF, the DTE should not transfer data across TxD.

TABLE C-1 Serial Port Pinouts *(Continued)*

Pin	Mnemonic	Signal Name	Description
6	DSR	Data Set Ready	Used by the DCE to indicate if it is ready to operate. When DSR is ON, the DCE is connected to the line and ready to exchange further control signals to start data transfer.
7	Gnd	Signal Ground	
8	DCD	Data Carrier Detect	Used by the DCE to indicate it is receiving a suitable signal from the communications channel.
9		Not connected	None.
10		Not connected	None.
11		Not connected	None.
12		Not connected	None.
13		Not connected	None.
14		Not connected	None.
15	TRxC	Transmit Clock	Used by the DCE to provide timing information to the DTE. The DTE provides data on TxD in which the transition of the bit corresponds to the rising edge of the clock.
16		Not connected	None.
17	RTxC	Receive Clock	Used by the DCE to provide timing information to the DTE. The falling edge of the clock corresponds to the center of the data bit received on RxD.
18		Not connected	None.
19		Not connected	None.
20	DTR	Data Terminal Ready	Used to control switching of the DCE to the communication channel. Once disabled, DTR cannot be enabled until SYNC is turned off.
21		Not connected	None.
22		Not connected	None.
23		Not connected	None.

TABLE C-1 Serial Port Pinouts *(Continued)*

Pin	Mnemonic	Signal Name	Description
24	TxC	Terminal Clock	Generated by the DTE to provide timing information to the DCE. Used only in synchronous mode and only when the driver requests a locally generated clock. Otherwise, TxC echoes the modem-generated clock. The falling edge of the clock corresponds to the center of the data bit transmitted on TxD.
25		Not connected	None.

C.3 Twisted-Pair Ethernet Connector

The twisted-pair Ethernet (TPE) connector is a RJ45 type connector located on the system board back panel. FIGURE C-3 illustrates the TPE connector configuration and TABLE C-2 lists the connector pin assignments.

Caution – Connect only a TPE cable into TPE connector.

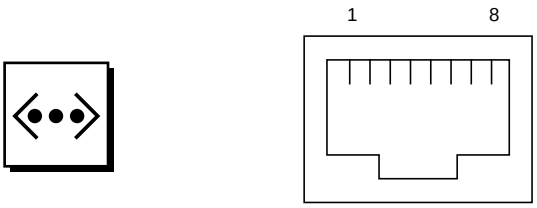


FIGURE C-3 TPE Socket

TABLE C-2 TPE Connector Pin Assignments

Pin	Signal Name	Description
1	tpe0	Transmit data +
2	tpe1	Transmit data –
3	tpe2	Receive data +
4	Common mode termination	Termination
5	Common mode termination	Termination
6	tpe3	Receive data –
7	Common mode termination	Termination
8	Common mode termination	Termination

C.4 Wide SCSI Connector

The wide small computer system interface (SCSI) connector is located on the system board back panel. FIGURE C-4 illustrates the wide SCSI connector configuration and TABLE C-3 lists the connector pin assignments.

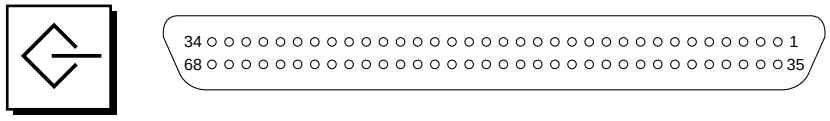


FIGURE C-4 Wide SCSI Connector Pin Configuration

TABLE C-3 Wide SCSI Connector Pin Assignments

Pin	Signal Name	Description
1	Gnd	Ground
2	Gnd	Ground
3	Gnd	Ground
4	Gnd	Ground
5	Gnd	Ground
6	Gnd	Ground
7	Gnd	Ground
8	Gnd	Ground
9	Gnd	Ground
10	Gnd	Ground

TABLE C-3 Wide SCSI Connector Pin Assignments *(Continued)*

Pin	Signal Name	Description
11	Gnd	Ground
12	Gnd	Ground
13	Gnd	Ground
14	Gnd	Ground
15	Gnd	Ground
16	Gnd	Ground
17	Termpower	Termpower
18	Termpower	Termpower
19	Not used	Undefined
20	Gnd	Ground
21	Gnd	Ground
22	Gnd	Ground
23	Gnd	Ground
24	Gnd	Ground
25	Gnd	Ground
26	Gnd	Ground
27	Gnd	Ground
28	Gnd	Ground
29	Gnd	Ground
30	Gnd	Ground
31	Gnd	Ground
32	Gnd	Ground
33	Gnd	Ground

TABLE C-3 Wide SCSI Connector Pin Assignments *(Continued)*

Pin	Signal Name	Description
34	Gnd	Ground
35	Dat<12>_	Data 12
36	Dat<13>_	Data 13
37	Dat<14>_	Data 14
38	Dat<15>_	Data 15
39	Par1 l_	Parity 1
40	Dat<0>_	Data 0
41	Dat<1>_	Data 1
42	Dat<2>_	Data 2
43	Dat<3>_	Data 3
44	Dat<4>_	Data 4
45	Dat<5>_	Data 5
46	Dat<6>_	Data 6
47	Dat<7>_	Data 7
48	Par0 l_	Parity 0
49	Gnd	Ground
50	Term_dis_	Term disable
51	Termpower	Termpower
52	Termpower	Termpower
53	Not used	Undefined
54	Gnd	Ground
55	Atn_	Attention
56	Gnd	Ground

TABLE C-3 Wide SCSI Connector Pin Assignments *(Continued)*

Pin	Signal Name	Description
57	Bsy_	Busy
58	Ack_	Acknowledge
59	Rst_	Reset
60	Msg_	Message
61	Sel_	Select
62	Cd_	Command
63	Req_	Request
64	IO_	In / Out
65	Dat<8>_	Data 8
66	Dat<9>_	Data 9
67	Dat<10>_	Data 10
68	Dat<11>_	Data 11

Note: _ (underscore) signifies active low

C.5 Alarm Connector

The alarm connector is located on the alarm card. This connector is a male DB-15 and TABLE C-4 lists each connector line assignment.

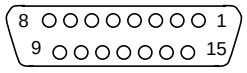


FIGURE C-5 Alarms Connector Configuration

TABLE C-4 Alarm Connector Pin Assignments

Pin	Signal Name	Pin	Signal Name
1	RESET+	9	ALARM1 COM
2	RESET–	10	ALARM1 NC
3	Not connected	11	ALARM2 NO
4	Not connected	12	ALARM2 COM
5	ALARM3 COM	13	ALARM2 NC
6	ALARM3 NO	14	Not connected
7	ALARM3 NC	15	Not connected
8	ALARM1 NO		

C.6 Media-Independent Interface Connector

The media-independent interface (MII) connector is located on the system board back panel. FIGURE C-6 illustrates the MII connector configuration and TABLE B-9 lists the connector pin assignments.

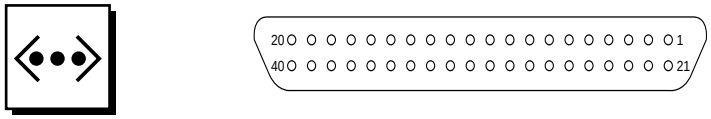


FIGURE C-6 MII Connector Pin Configuration

TABLE C-5 MII Connector Pin Assignments

Pin	Signal Name	Description
1	Pwr	Power
2	Mdio	Management data I/O
3	Mdc	Management data clock
4	Rxd3	Receive data 3
5	Rxd2	Receive data 2
6	Rxd1	Receive data 1
7	Rxd0	Receive data 0
8	Rx dv	Receive data valid
9	Rx clk	Receive clock
10	Rx er	Receive error
11	Tx er	Transmit error

TABLE C-5 MII Connector Pin Assignments *(Continued)*

Pin	Signal Name	Description
12	Tx clk	Transmit clock
13	Tx en	Transmit data enable
14	Txd0	Transmit data 0
15	Txd1	Transmit data 1
16	Txd2	Transmit data 2
17	Txd3	Transmit data 3
18	Col	Collision detected
19	Crs	Carrier sense
20	Pwr	Power
21	Pwr	Power
22	Gnd	Ground
23	Gnd	Ground
24	Gnd	Ground
25	Gnd	Ground
26	Gnd	Ground
27	Gnd	Ground
28	Gnd	Ground
29	Gnd	Ground
30	Gnd	Ground
31	Gnd	Ground
32	Gnd	Ground
33	Gnd	Ground
34	Gnd	Ground

TABLE C-5 MII Connector Pin Assignments *(Continued)*

Pin	Signal Name	Description
35	Gnd	Ground
36	Gnd	Ground
37	Gnd	Ground
38	Gnd	Ground
39	Gnd	Ground
40	Pwr	Power

C.7 Parallel Interface

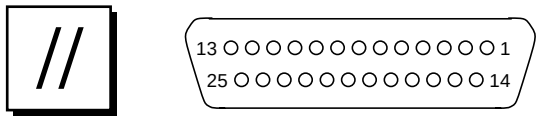


FIGURE C-7 DB-25 Parallel Connector

TABLE C-6 Parallel Connector Pinouts

Pin	Description	Pin	Description
1	Data_Strobe_L	14	AFXN_L
2	Data0	15	ERROR_L
3	Data1	16	RESET_L
4	Data2	17	IN_L
5	Data3	18	Ground
6	Data4	19	Ground
7	Data5	20	Ground
8	Data6	21	Ground
9	Data7	22	Ground
10	ACK_L	23	Ground
11	BUSY	24	Ground
12	PERROR	25	Ground
13	SELECT_L		

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