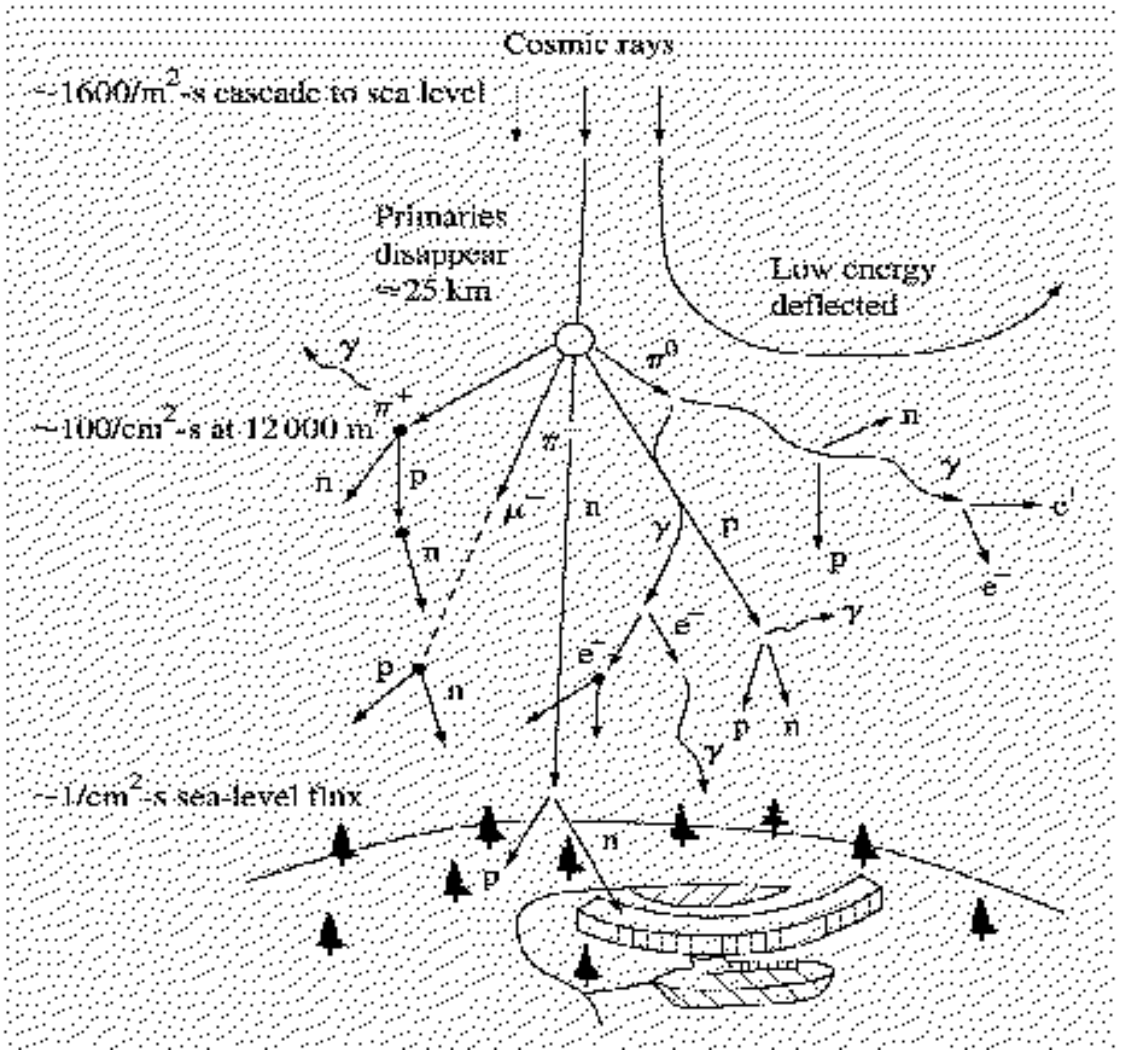
How Cosmic Rays Cause Computer Downtime

Ray Heald

Sun Microsystems

Cosmic Ray Particle Generation



J.F. Ziegler, IBM [A1] .

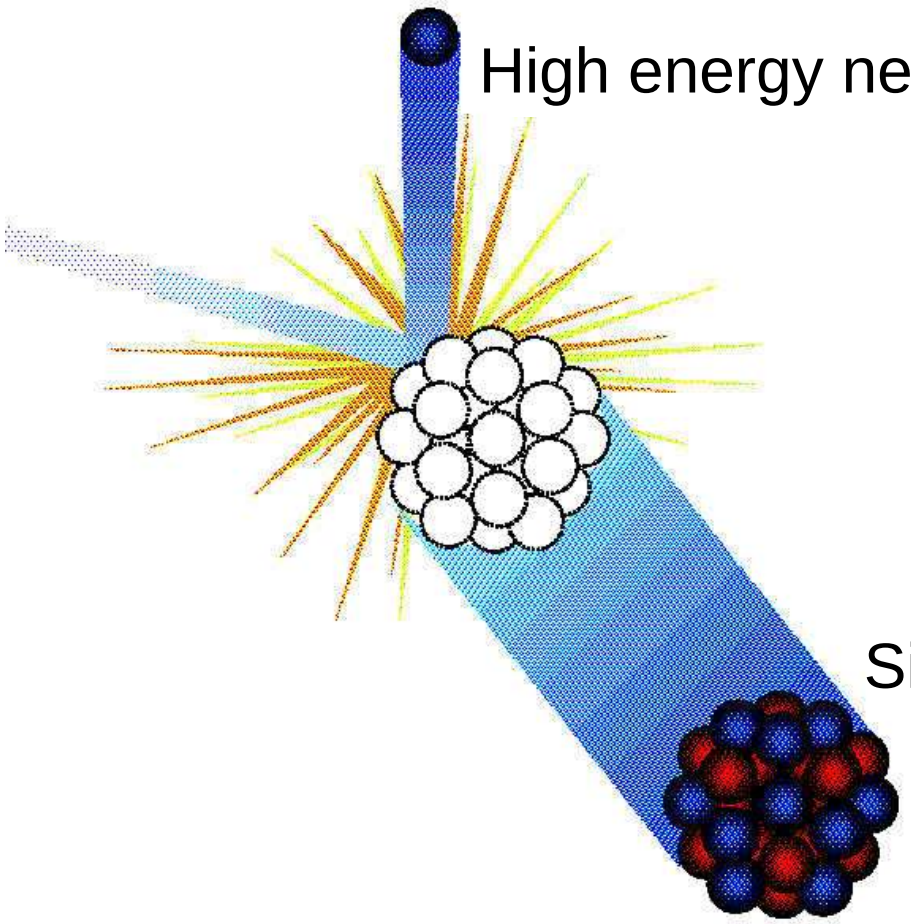
Outer Space Cosmic Particles

92% protons
6% alphas
1% heavy nuclei
Energies up to 10^{19} eV
from Supernova explosions, pulsars, & galactic explosions.

Sea Level Cosmic Particles Causing IC Upsets

96% neutrons
<1% primary particles
(~0% solar cosmic)
Energies up to 10^{11} eV

Elastic Energy Transfer in Silicon

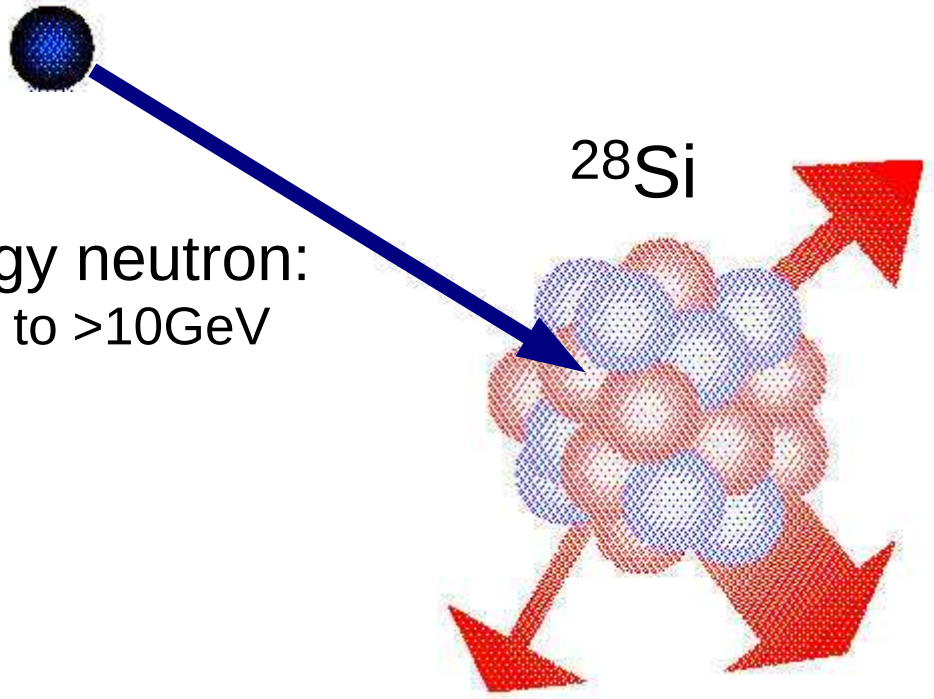


Energy and momentum from cosmic caused neutron can be transferred to a silicon or other IC nucleus.

Maximum recoil energy is 13.3-13.6% of incident neutron. For incident neutron of 100MeV => range up to 5μ (most < 2μ).

R. Baumann, Texas Instruments [1]

Inelastic Energy Transfer in Silicon



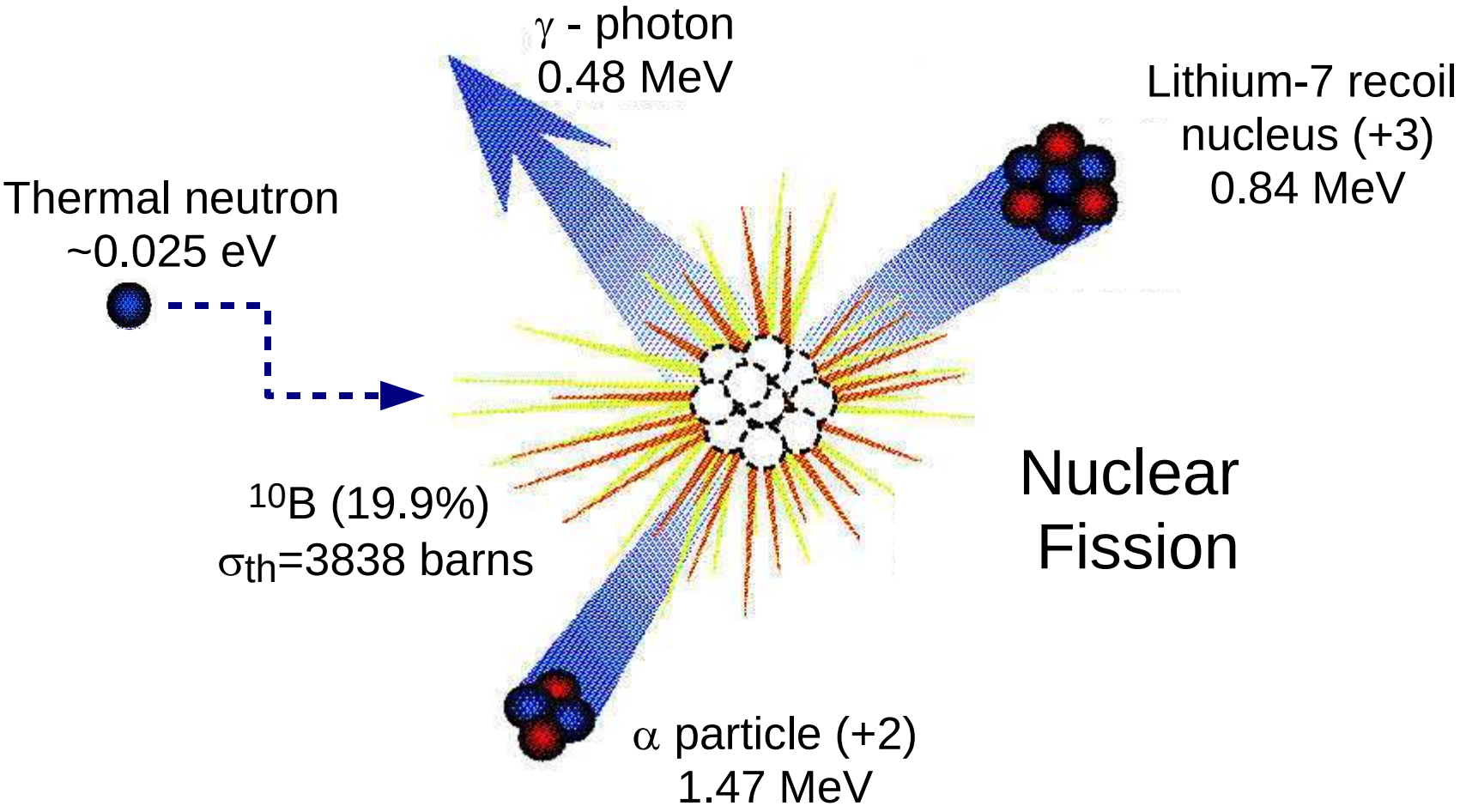
High energy neutron:
~100 MeV to >10GeV

Burst of electronic charge

^{28}Si nucleus fragments:
pions, *n*, *p*, ^{2}H, ^{3}H, ^{4}He, & other light ions receive energy from incident neutron.

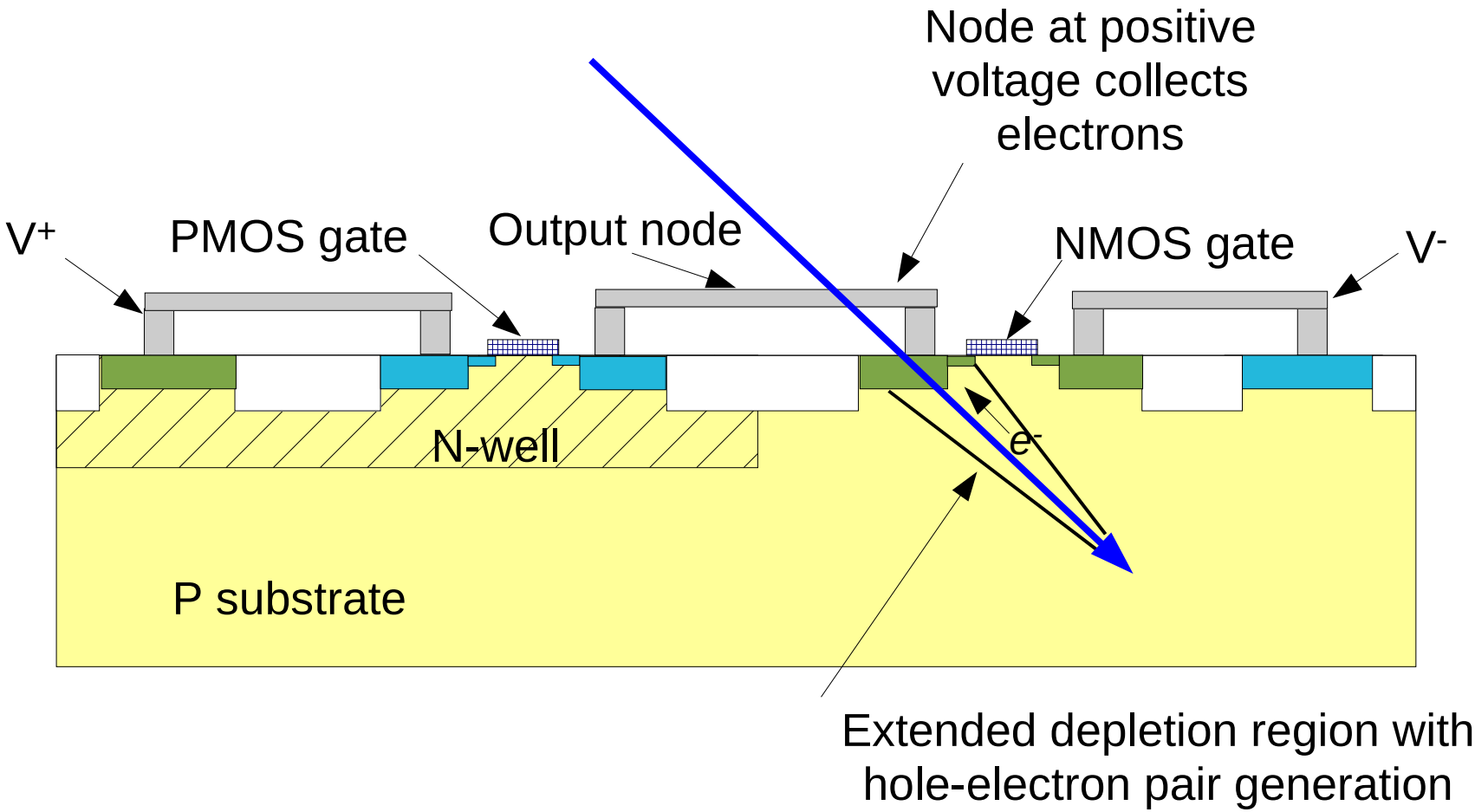
R. Baumann, Texas Instruments [1]

Thermal Neutron Interaction with Boron-10



R. Baumann, Texas Instruments [1]

Charged Particle Transferring Charge to Circuit Node



Flow of the Talk

- Motivation
- Soft error history: Alpha particles in silicon ICs.
  - DRAM soft error problems of the 70s.
  - Circuit & processing/packaging recovery techniques of the 80s.
  - Alpha particles from flip chip solder balls of the 90s.
  - Circuit & processing solutions for flip chip alpha particles.
- Cosmic SER
  - SRAM & Logic soft error victims.
  - Measurement and recovery techniques.
- SEL & SEU in the future

Soft Errors in 70s DRAMs

The Problem: Soft errors caused DRAM board failures.

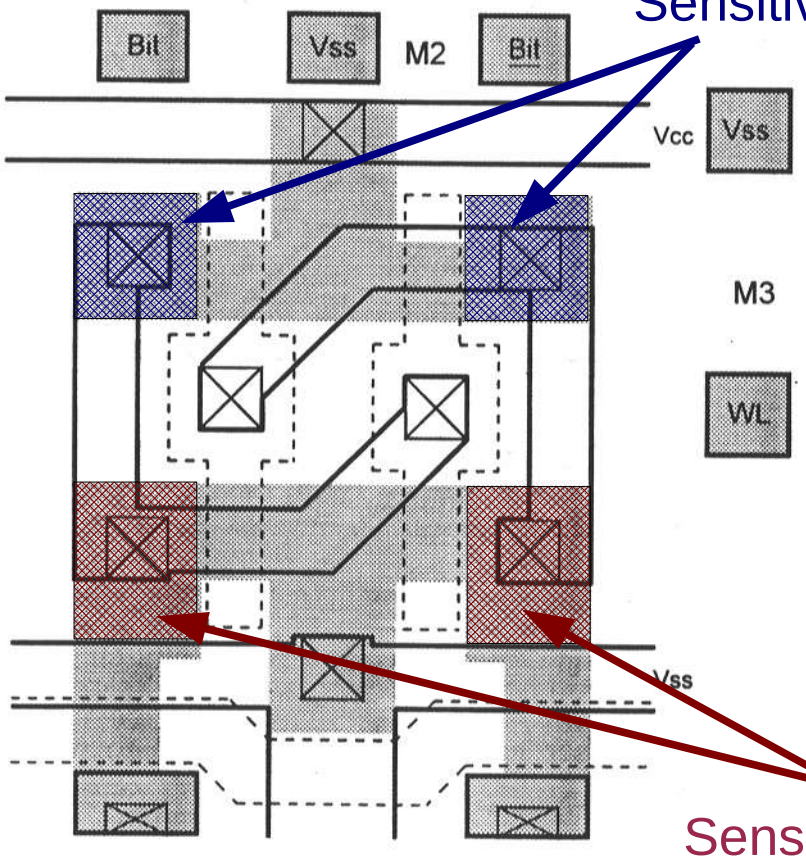
- In 1978 May and Woods reported "A New Physical Mechanism for Soft Errors in Dynamic Memories" and in 1979, "Alpha-Particle-Induced Soft Errors in Dynamic Memories."
- Alpha particles (^{4}He nuclei, charge of +2) result from the decay of minute concentrations of radioactive isotopes in ICs.
  - Natural alpha sources: ^{238}U and ^{232}Th decay chains.
  - Birth energies: 4 MeV to 9 MeV (track length up to 65μ).
  - Energy transfer: ~1 electron-hole pair per 3.6 eV energy loss.
  - Minority carrier collection: Charge transfer is up to 400 fC.
- DRAMs most sensitive; SRAMs saw problem ~2 years later.

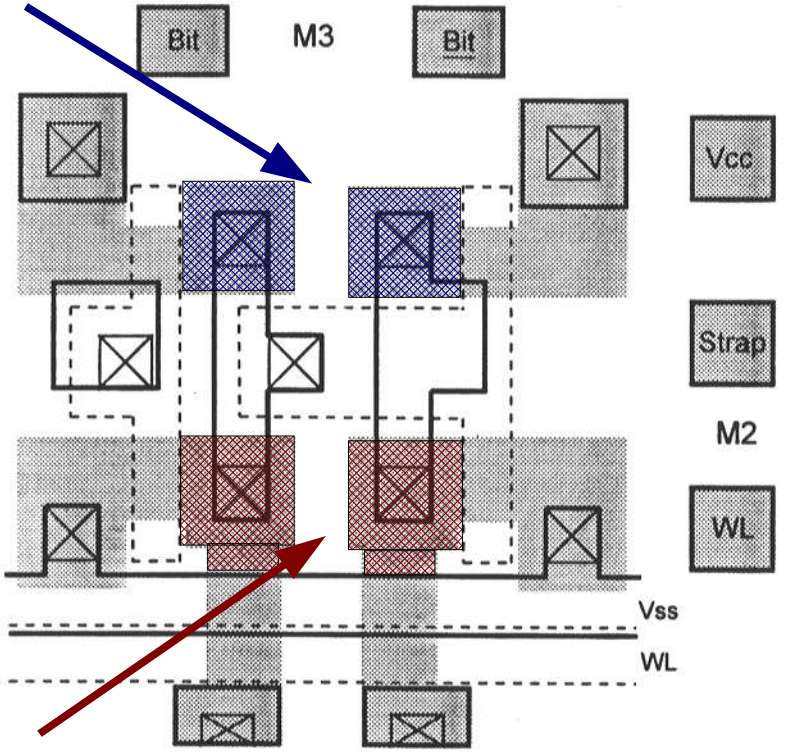
Memory Cell Layout Examples*

2nd Metal Bitline Memory Cell

3rd Metal Bitline Memory Cell

Sensitive PMOS diffusion areas

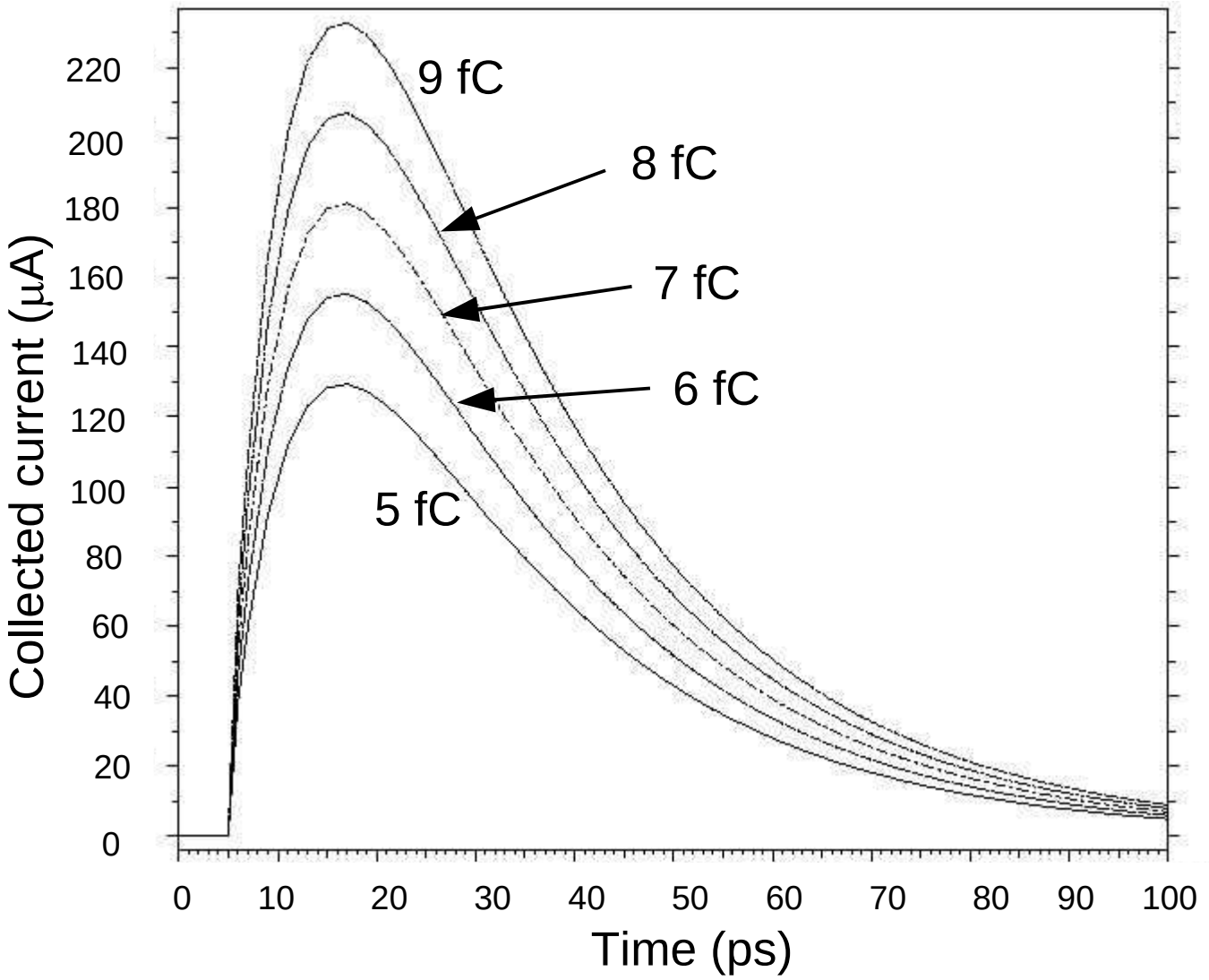




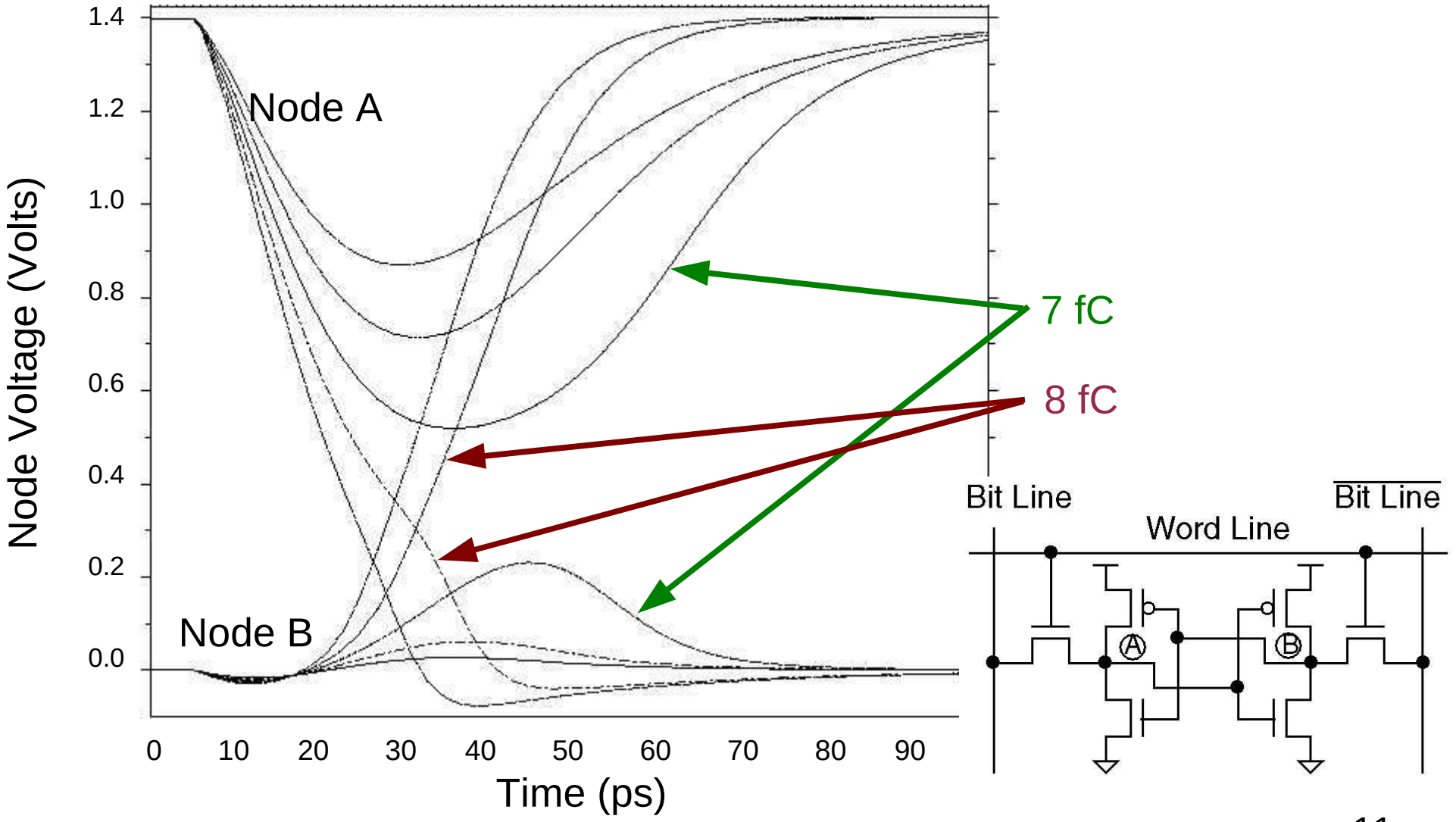
Sensitive NMOS diffusion areas

* Bohr and El-Mansy, Intel [2].

Current Waveforms Generated from Alpha Particles



Charged Particle Memory Cell Interaction: Q_{crit} ~7.5 fF



Alpha Problem in Silicon ICs

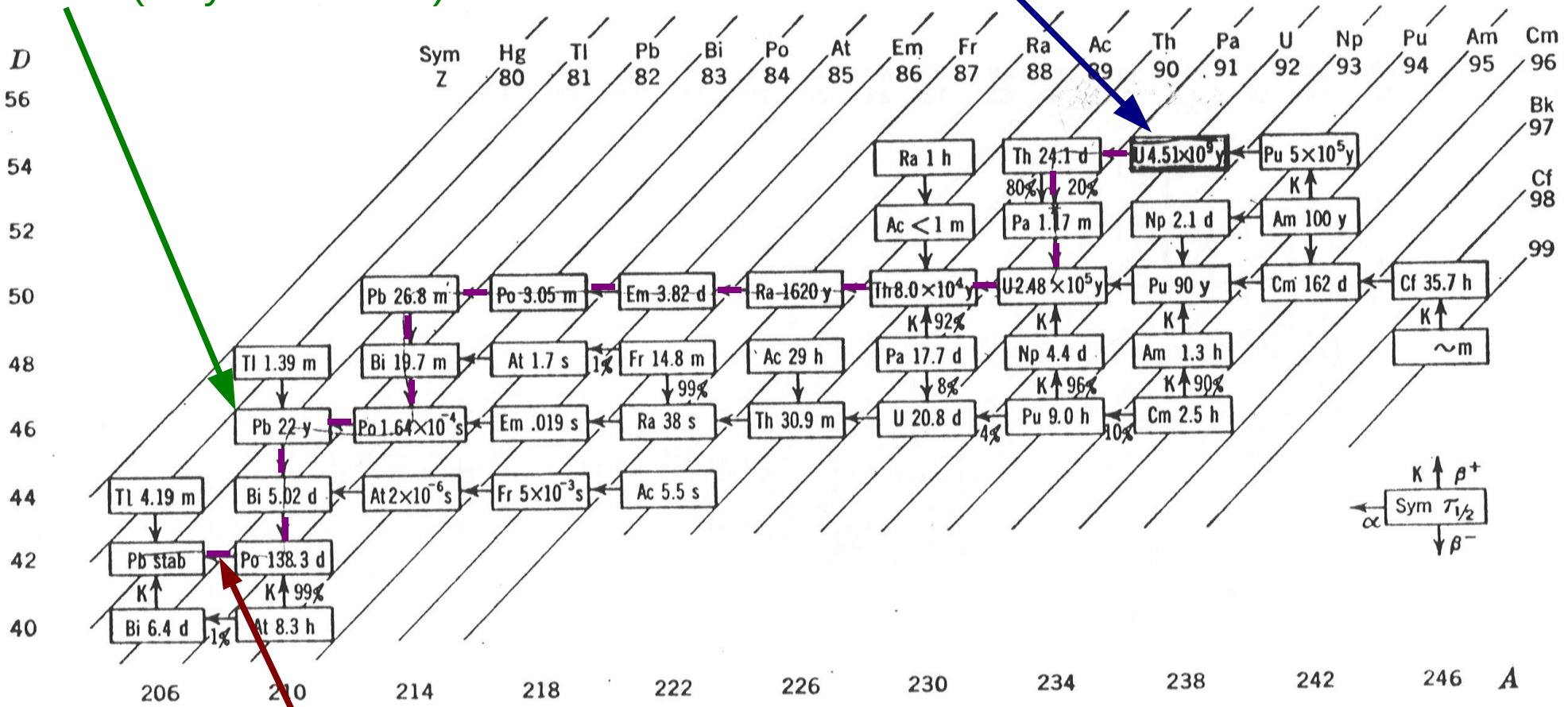
Where did it come from?

- Sources include: Ceramic package materials, aluminum IC interconnect, and lead in solder bump material.
- Ceramic package contamination due to uranium and thorium impurities in package material and lid attach glass.
- Aluminum contamination due to uranium and thorium impurities in aluminum ore.
- Lead contamination due to uranium and thorium impurities in lead ore including the radioactive lead decay products ^{210}Pb and ^{212}Pb.

Heavy Metal Members of the 4n+2* Radioactive Family

^{210}Pb (22 year half life)

^{238}U (4.5×10^9 year half life)



^{210}Po => ^{206}Pb + 5.3MeV α

* ^{238}U series: Others are ^{237}Np (2.2×10^6 yr.), ^{235}U (8.52×10^8 yr.), and ^{232}Th (1.39×10^{10} yr.). A. E. S. Green, *Nuclear Physics* [3].

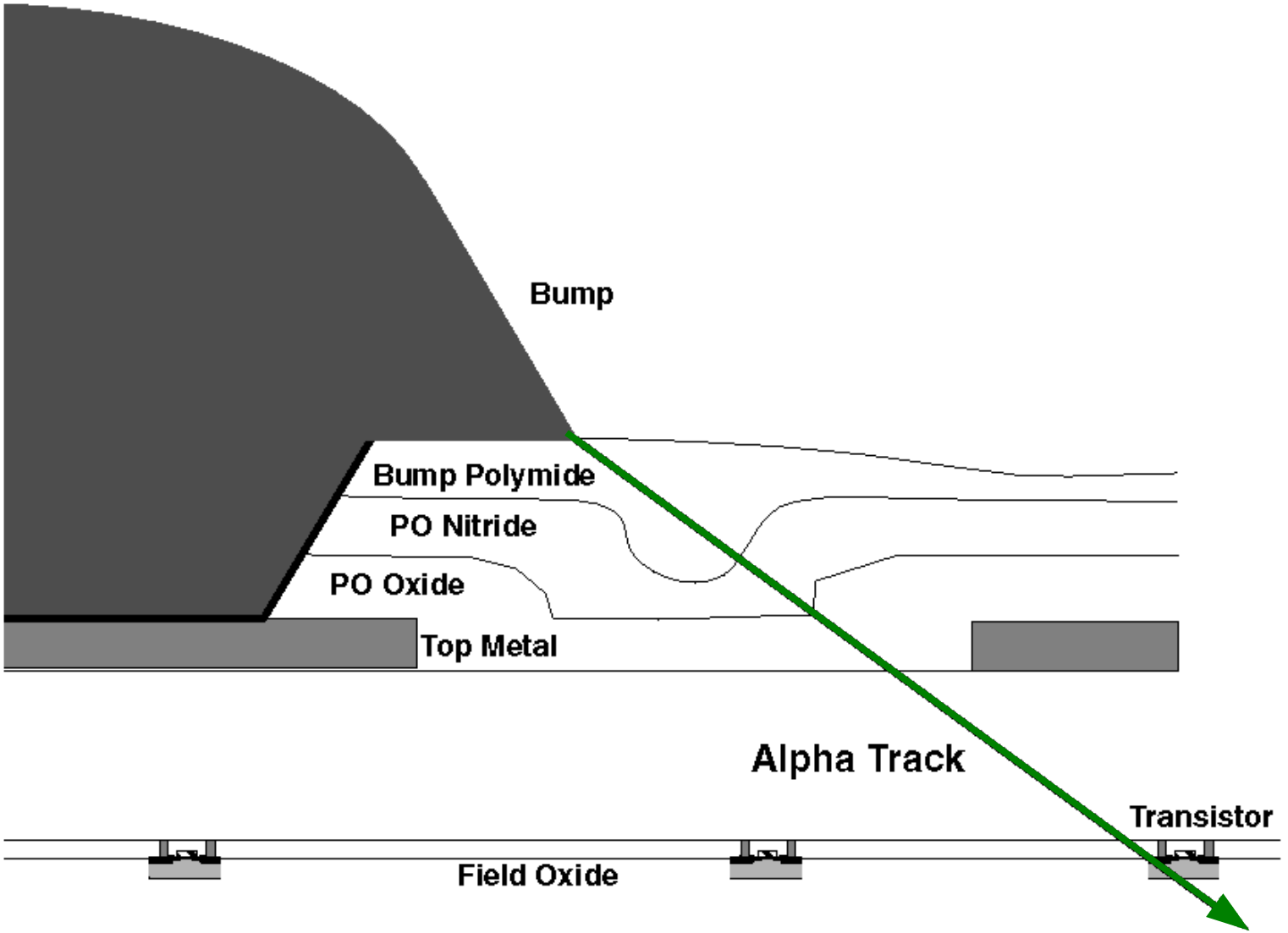
Protection Techniques of the 80s

- High capacitance:
  - Maximum charge collected from a single terrestrial alpha particle event is 400 fC; node capacitance of over 240 fF needed to maintain state (with a 3.3 V supply and a trip point of 1.65 V).
  - Expected charge collected from a single alpha particle event is 100 fC; node capacitance of 60 fF needed to maintain state.
- Remove alpha sources:
  - High purity aluminum
  - Plastic packages
- Protect the circuit with die coatings in ceramic packages. Polyimide thickness > 50μ => alpha SER reduction of 98%.

The 90s: Alpha Particles from Lead Flip-Chip Solder Balls

- Lead in solder contains ^{210}Pb and other members of the ^{238}U and ^{232}Th decay chains.
- $^{210}Pb \Rightarrow {}^{210}Bi + \beta- \Rightarrow {}^{210}Po + \beta- \Rightarrow {}^{206}Pb + \alpha$
- Resultant alpha particle energy = 5.3 MeV - Half Life 22 years.
- Maximum charge generated ~236 fC in a track length of about 28 μ.
- Node capacitance of 145 fF needed to maintain state (with a 3.3 V supply and a trip point of 1.65 V).

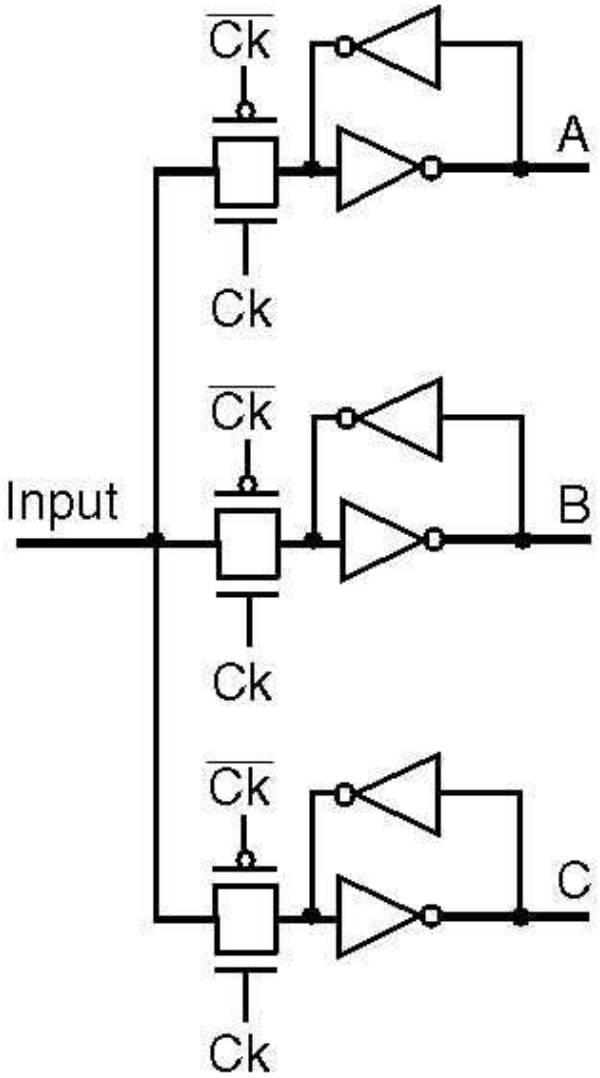
Alpha Track From Bump Through a Transistor

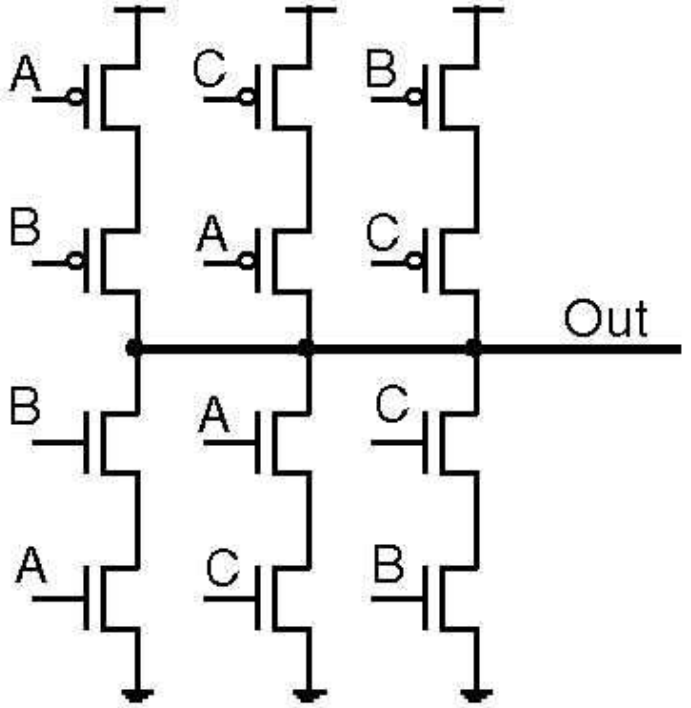


Circuit Techniques Near Solder Balls

- Keep out zones - ~40μ from sensitive device.
- High capacitance - ~150 fF with 3.3V supply and 1.65V trip.
- High drive current
  - Static circuits require ~2mA hold current (~8μ PMOS in 0.25μ process).
  - Alpha hit which does not change the logic level may still increase circuit delay.
- Majority vote circuits

Simple Majority Vote Circuit





SRAM α SER Limitations

- SRAM disturb charge very small: $Q_{crit\text{-}SRAM} < Q_{crit\text{-}DRAM}$.
- SRAM memory cell cannot be made alpha hard in an acceptable area with standard processing.
  - 6 transistor SRAM cells for 90nm processes are about $1\mu^2$ in area. This is the expectation to keep up with Moore's Law.
  - 6T memory cell may contain < 5 fC.
  - Alpha particle energy loss results in charge of 5 fC in < 1 μ.
- Bit lines and sense amplifiers are also alpha sensitive for 25-50% of cycle.
- Circuit level solutions:
  - DRAM style: High capacitance areas added above memory cells for reduced SER at added processing cost and slower write times.
  - Protect with parity or ECC.

Processing Solutions for the Solder Ball Alpha Particle Problem

- Aged lead - ^{210}Pb half life is 22 years
- Isotope refined lead - Laser refinement and other techniques are now available
- Lead free solder - copper, silver, and tin material: CuAgSn
- Gold solder balls

Caution - Lead free does not necessarily mean radiation free. All materials must be sufficiently low alpha emissivity after all manufacturing is complete to limit alpha caused soft errors.

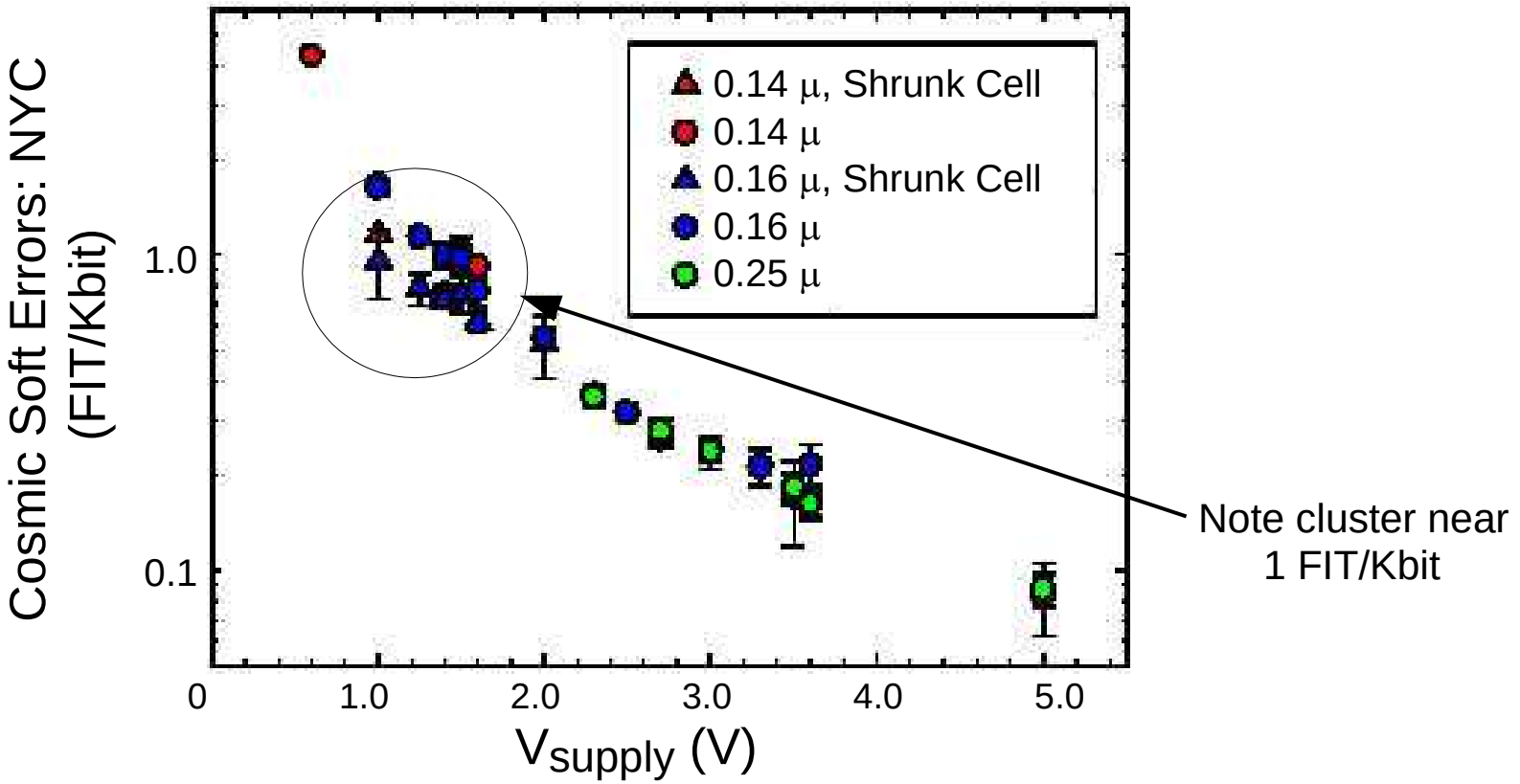
Typical Alpha Flux in IC Materials (α/cm^2-hr)

Processed wafers	0.0009
Copper interconnect metal	0.0019
Aluminum interconnect metal	0.0014
Mold compound	0.024 - <0.002
Underfill	0.002 - 0.0009
Lead solder bumps	7.2 - <0.002
Ceramic package	0.0011

Ziegler & Puchner, Cypress Semiconductor [B].

Cosmic Soft Errors vs. Technology & Voltage

Cosmic events are the dominate cause of soft errors in ICs manufactured with very low alpha materials.



P.E. Dodd, et. al., Sandia [4].

Cosmic SER Sources

- Primary cosmic rays are high energy particles from outer space which entry the solar system and may hit the earth.
- Many interactions occur in the atmosphere resulting in the cascade of secondary particles which reach the surface of the earth.
- "The relative SER importance of the various particles at sea level (neutrons, protons, pions, muons, electrons, and photons) is understood. Neutrons are the primary problem."*

* J.F. Ziegler, IBM [A2].

Cosmic Neutron Properties

- Cosmic neutrons properties are determined by the interactions of cosmic and secondary particles in the atmosphere:
  - Neutron energy range is to over 10000 MeV at the earth's surface.
  - Neutron intensity increases dramatically with altitude.
  - Neutron intensity also varies by ~2x with location on the earth.
  - A cosmic caused neutron can cause several charged particles.
  - 1 m concrete is needed to attenuate the *n* flux at sea level by 30%
- One of many possible cosmic caused events with a 200 MeV neutron interacting with silicon:*
  - $^{28}Si + n \Rightarrow 2n + 2p + {}^{25}Mg^*$ (excited state)
  - $^{25}Mg^* \Rightarrow {}^{12}C + 3\ {}^{4}He + n$
  - Six resultant charged fragments with energies from 4 to 12 MeV.

* H.H.K. Tang, IBM [A3].

Cosmic Neutron Caused Soft Errors

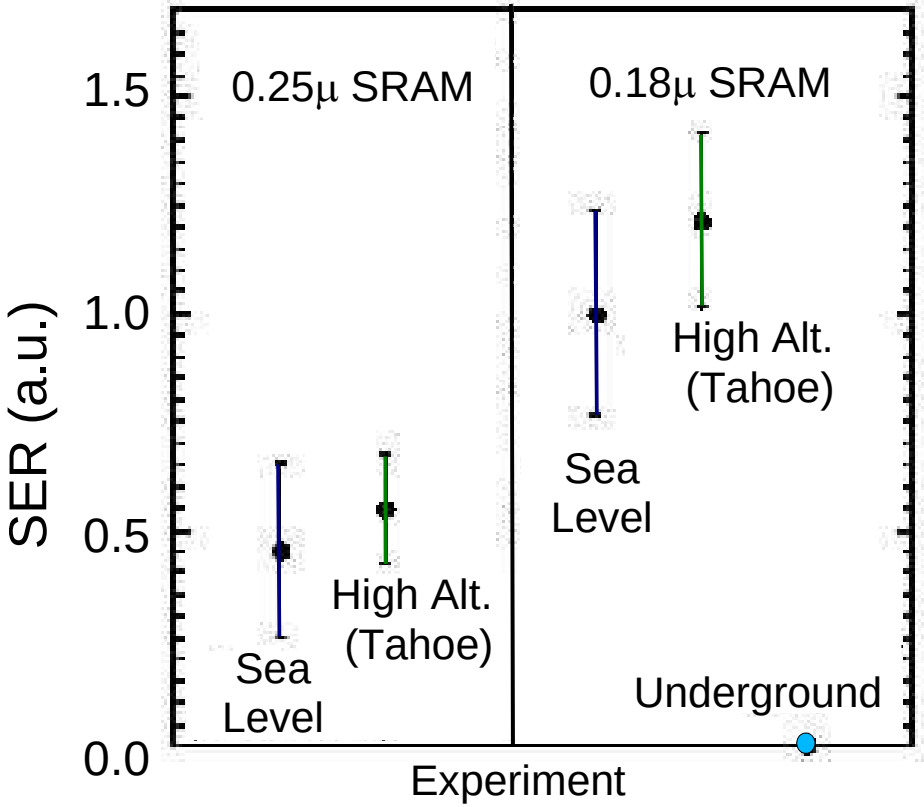
- High energy neutron interaction with SRAM memory cells:
  - Typical SRAM neutron induced SER ~1 kFIT/Mbit (1 FIT/Kbit) with 1-5% multicell upsets.
    - Up to ~0.5% of all neutron induced SE result in multicell errors accessed simultaneously.
    - Spacing of cells is critical to limit multibit errors in a single access.
  - 4MB (~38Mbit) SRAM => ~38000 FIT or ~0.32 fails/year without protection. With 1 bit ECC correction the uncorrected SER is less the 2000 FIT and less than 1 FIT with sufficient bit spacing.
- Thermal neutron generated α:
  - $^{10}B + n \Rightarrow {}^{7}Li + \alpha$ (1.48 MeV / range ~ 5.2 μ).
  - BPSG often used for oxide just after gate etch.

High Altitude Soft Error Test Results

- Testing at high altitude allows a 3 to 10x acceleration factor.

  Neutron flux increases about 1.3x for each 1000 ft. altitude to >10,000 ft.

- Testing can require months and thousands of devices under test.



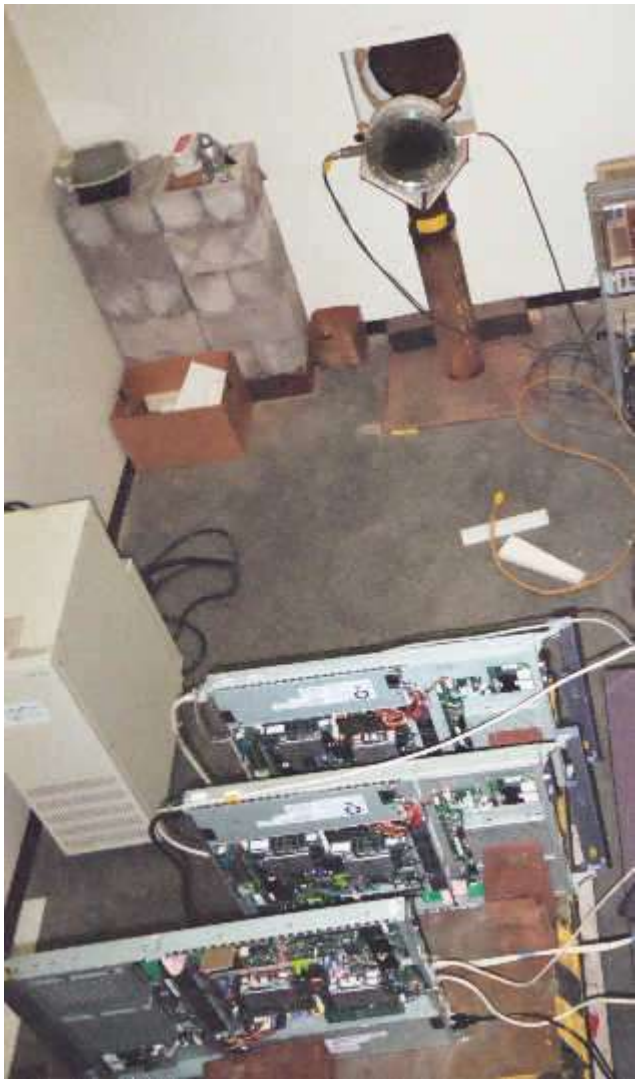
H. Kobayashi, et. al., Sony [5].

Computer High Altitude Tests

Space and time are needed for high altitude cosmic neutron SER testing.

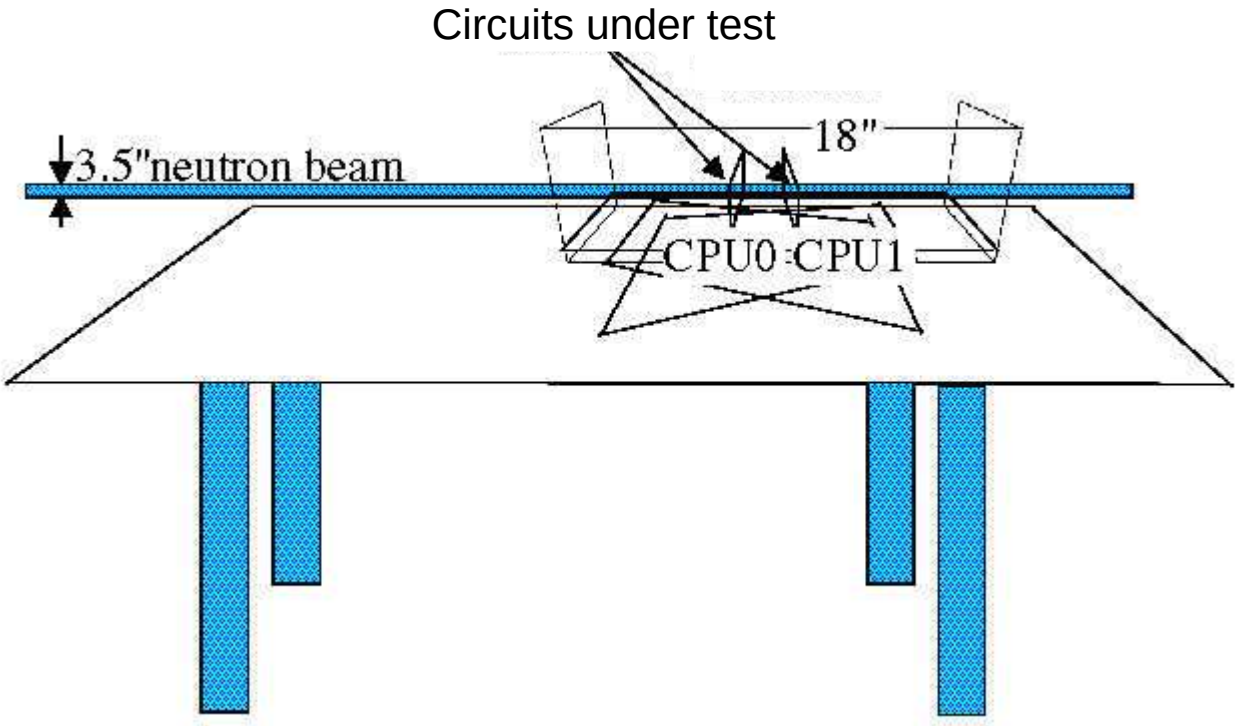
Los Alamos Neutron SER Tests

- Accelerated testing of computers is need to determine cosmic neutron SER.
- Los Alamos LANSCE site allows testing with an energy distribution very close to the cosmic neutron flux at the earth's surface and $2.5x10^8$ times the intensity.

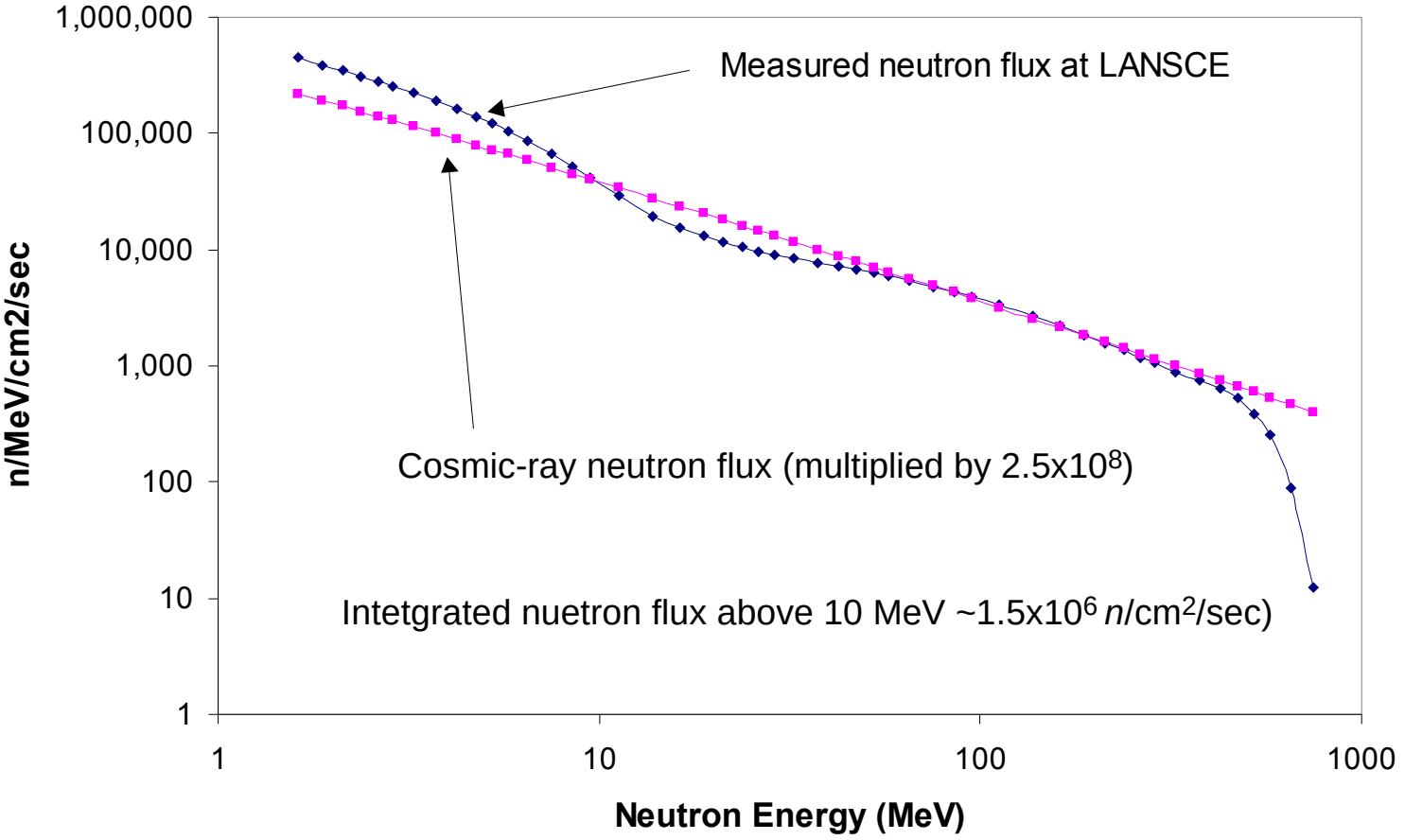


Los Alamos Neutron SER Tests-2

Setup is such that only a small section is tested at once allowing detailed information on individual circuits.



Los Alamos Neutron Flux



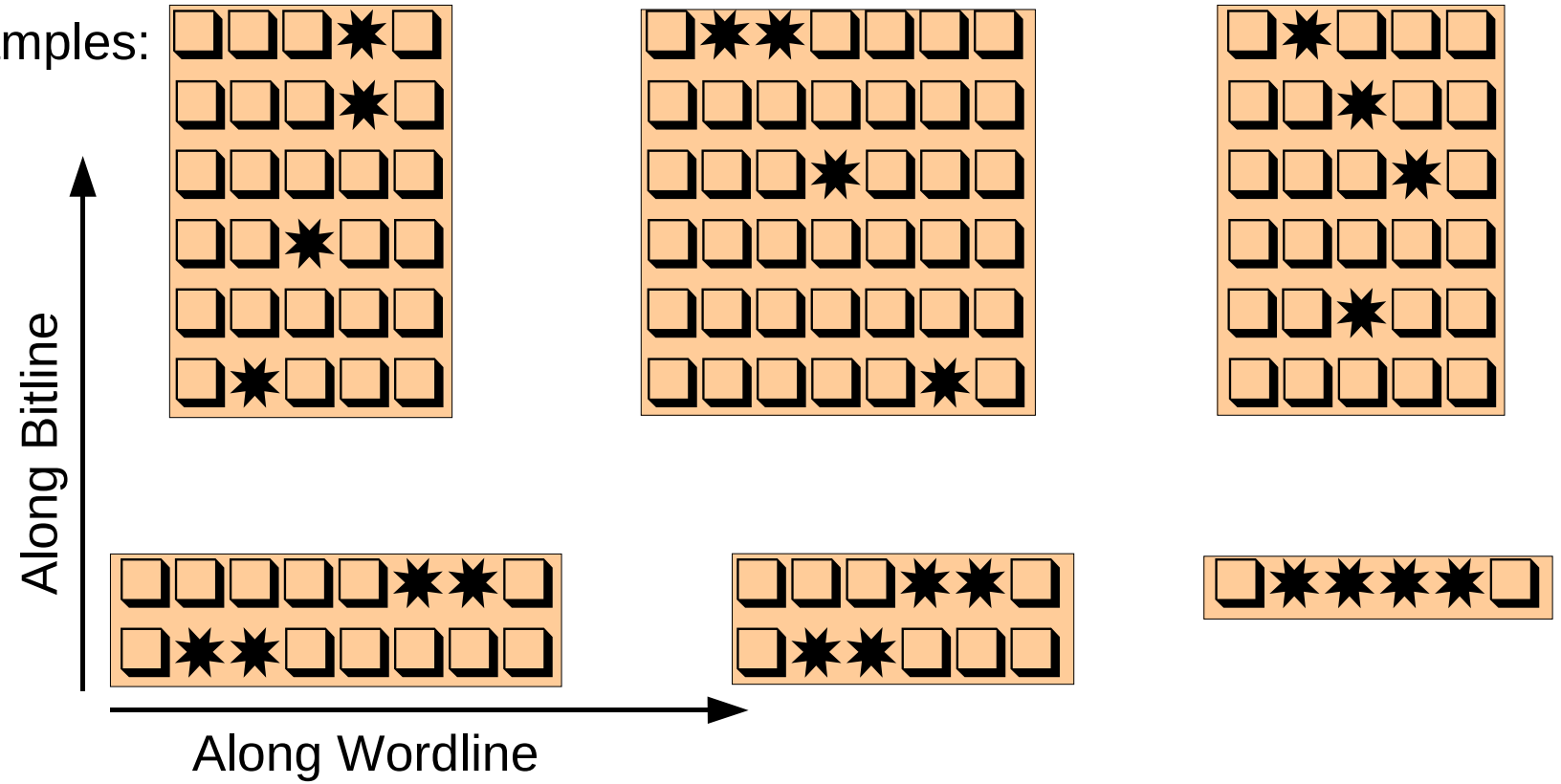
LANL beam spectrum closely resembles natural cosmic neutron flux.
Acceleration: 1 hour in beam = 28000 years of cosmic background.

* Wender, Los Alamos Nat. Lab. [6].

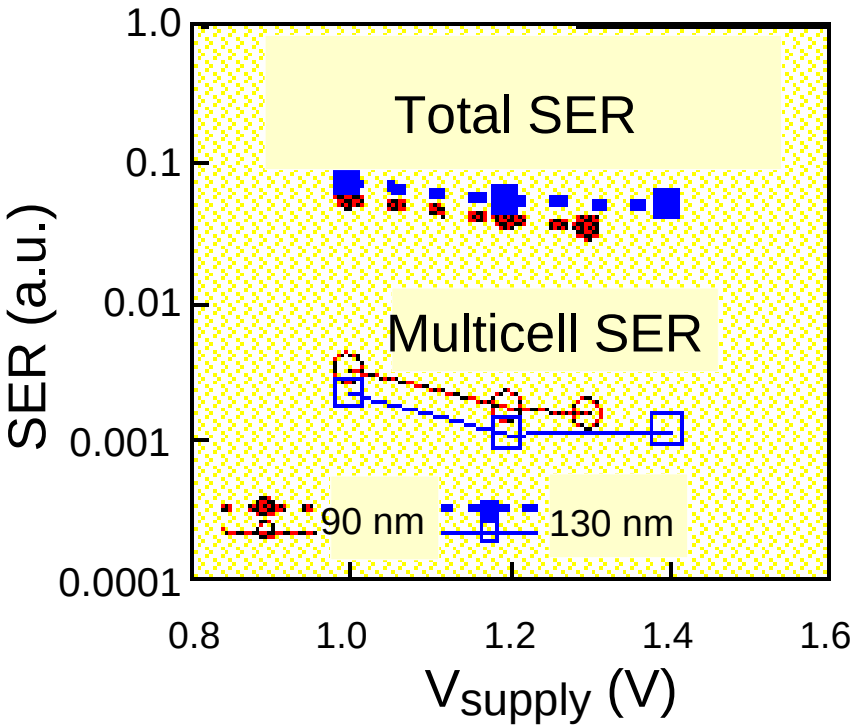
Multicell Soft Error Events

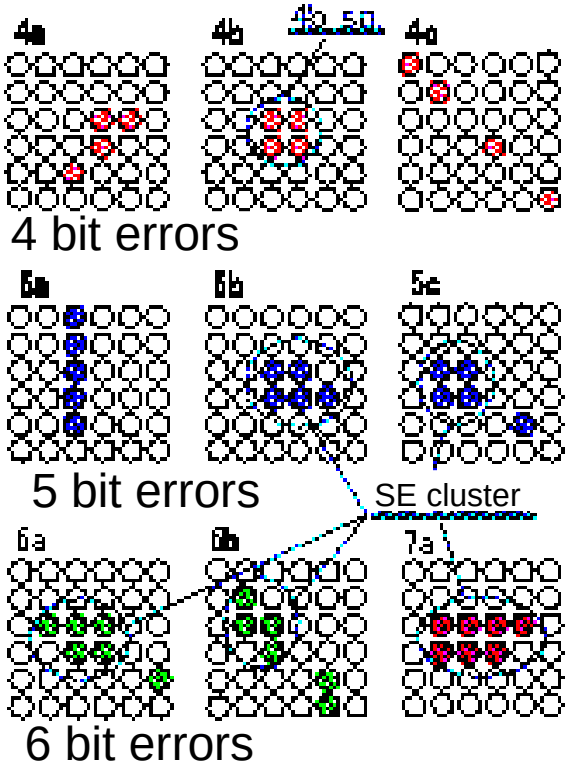
- For parity and ECC protected RAMs, multicell events including two or more cells in the same protected data block determine the system soft error failure rate.
- Accelerated testing shows care is needed to prevent multicell events from causing system failures.

Examples:



SRAM Multicell Soft Errors

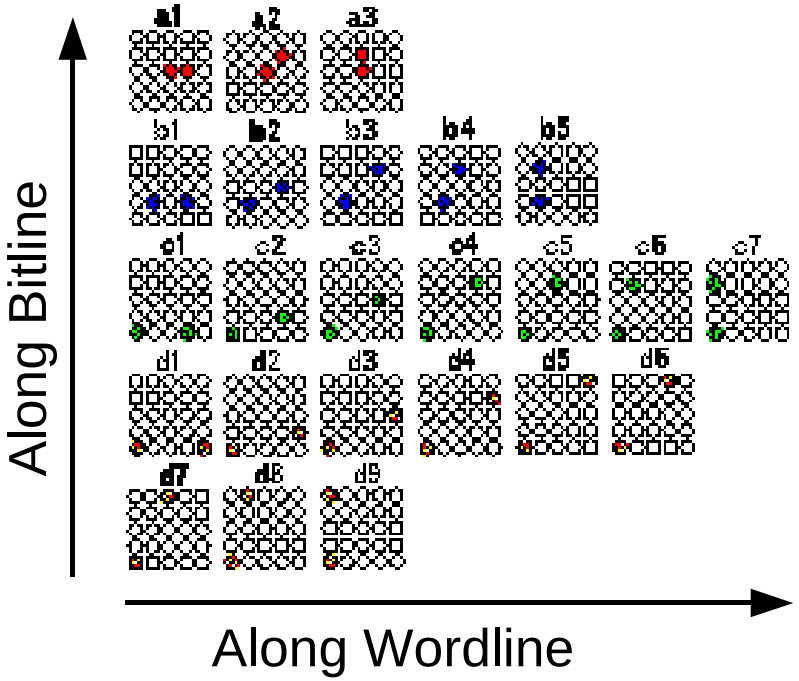


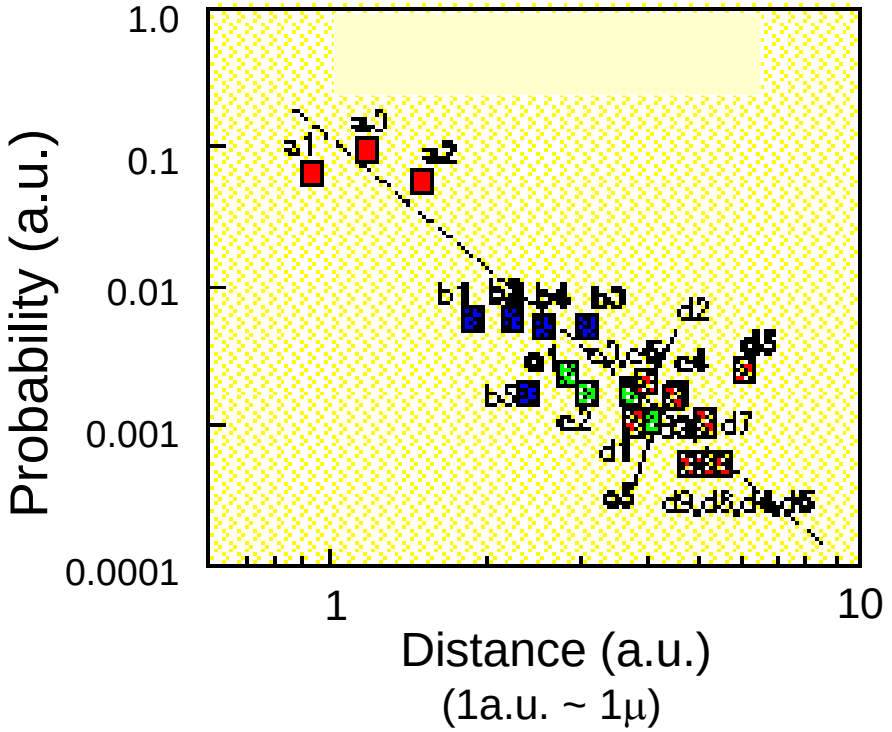


Y. Tosaka, et. al., Fujitsu [7].

Multicell Soft Errors with Position

2-bit soft errors relative positions in 90nm 1.2V SRAM





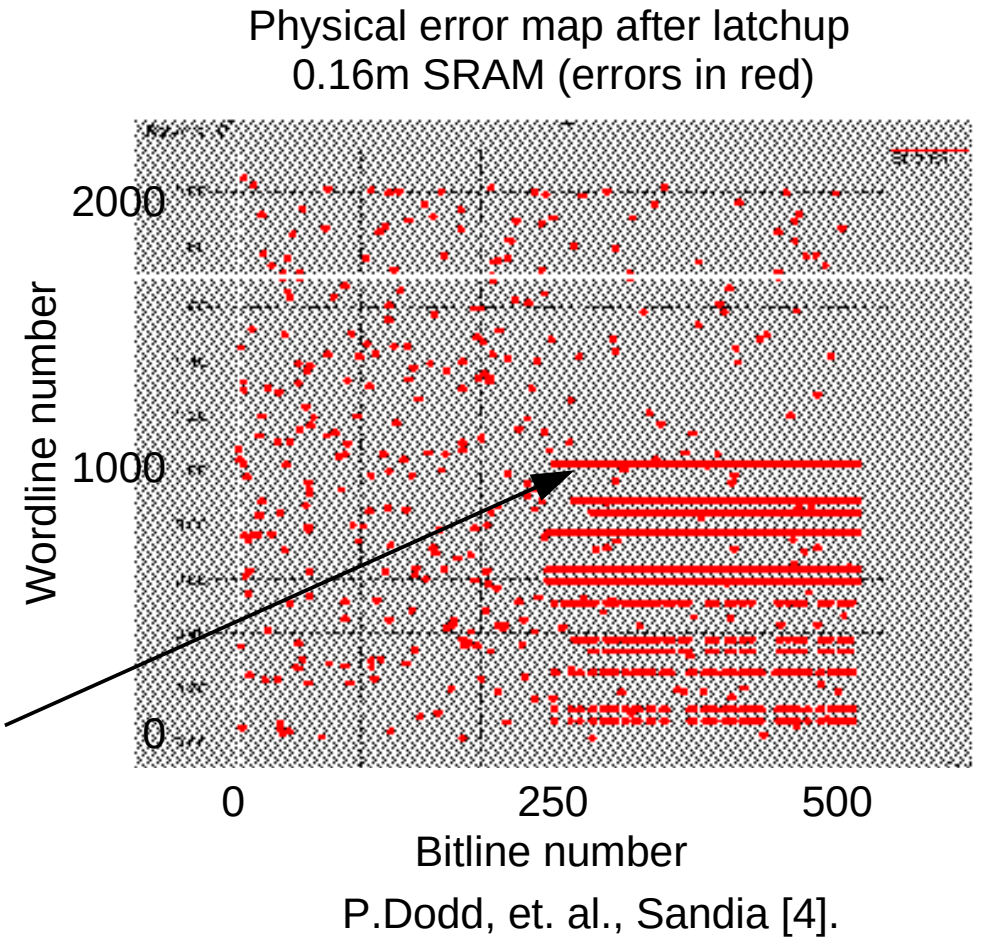
Y. Tosaka, et. al., Fujitsu [7].

Soft Error Latch-Up

- Soft error latch-up, SEL, is latch-up initiated by a single charged subatomic particle event.
  - Not related to total dose induced latch-up often seen in space applications.
  - Alternate name, Single Event Latch-up, stresses the single event nature.
- Characteristics of SEL
  - Region of SRAM or logic circuit does not operate (usually stuck in a state) and draws significantly higher than expected current.
  - Fault cannot be cleared by any circuit logical operation.
  - Power cycling removes fault.

Soft Error Latch-Up Example

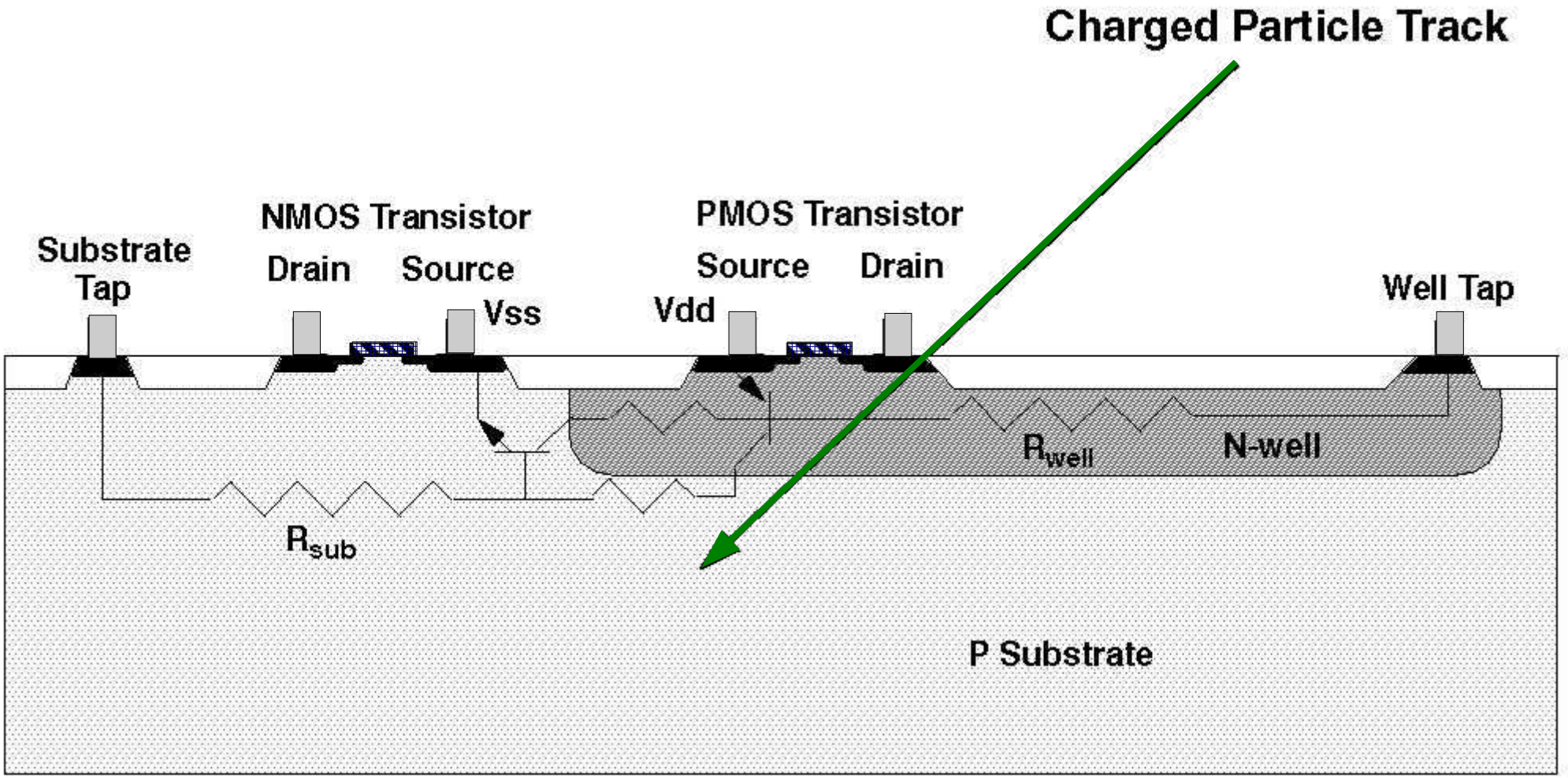
Accellerated test showing individual bit failures and single event latch-up



Red lines are stuck groups of cells (Probably pairs of wordlines).

P.Dodd, et. al., Sandia [4].

Cosmic Latch-up Circuit



Future

- Alpha Free Bump Material < 0.0002 $\alpha/cm^2/hr$.
- ECC or parity with reload (keep out zones for memory arrays are not useful once materials are alpha free).
- Much more protection of logic through residue checks and other low overhead data verification.
- Lockstep operation (and protect all non-duplicated stages).
- Cosmic particle induced soft errors interacting with unprotected cells of logic set practical limit.

References: Complete Topic

[A] *IBM J. Res. Develop*., vol. 40, no. 1, Jan. 1996.

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[A1] J.F. Ziegler et. al., "IBM experiments in soft fails in computer electronics," *IBM J. Res. Develop*., vol. 40, no. 1, Jan. 1996, p. 3-18.

[A2] J.F. Ziegler, "Terrestrial Cosmic Rays," *IBM J. Res. Develop*., vol. 40, no. 1, Jan. 1996, p. 19-39.

[A3] H.H.K. Tang, "Nuclear physics of cosmic ray interaction with semiconductor materials: Particle-induced soft errors from a physicist's perspective," *IBM J. Res. Develop*., vol 40, no. 1, Jan. 1996, p. 91-108.

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[3] A. E. S. Green, *Nuclear Physics*, New York: McGraw Hill Book Co. Inc., 1955, pp. 199-202.

[4] P. E. Dodd, et. al., “Neutron-Induced Soft Errors, Latchup, and Comparison of SER Test Methods for SRAM Technologies,” *IEDM Tech. Digest,* Dec. 2002, pp. 333-336.

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[6] Wender, “Neutron Radiation Effects in Semiconductor Devices and Systems,” *LANSCE-3, Neutron and Nuclear Science Group, Los Alamos Nat. Lab*., May 2000.

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Other Papers of Interest-1

Some Classic Alpha Papers

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B. Chappell, S. Schuster, G. Sai-Halasz, “Stability and SER Analysis of Static RAM Cells,” *IEEE J. Solid-State Circuits,* vol. 20, pp. 383-390, Feb. 1985.

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R. C. Baumann, T. Z. Hossain, S. Murata, H. Kitagawa, "Boron Compounds as a Major Source of Alpha Particles in Semiconductor Devices," *IEEE Proc. IRPS*, pp. 297-302, 1995.

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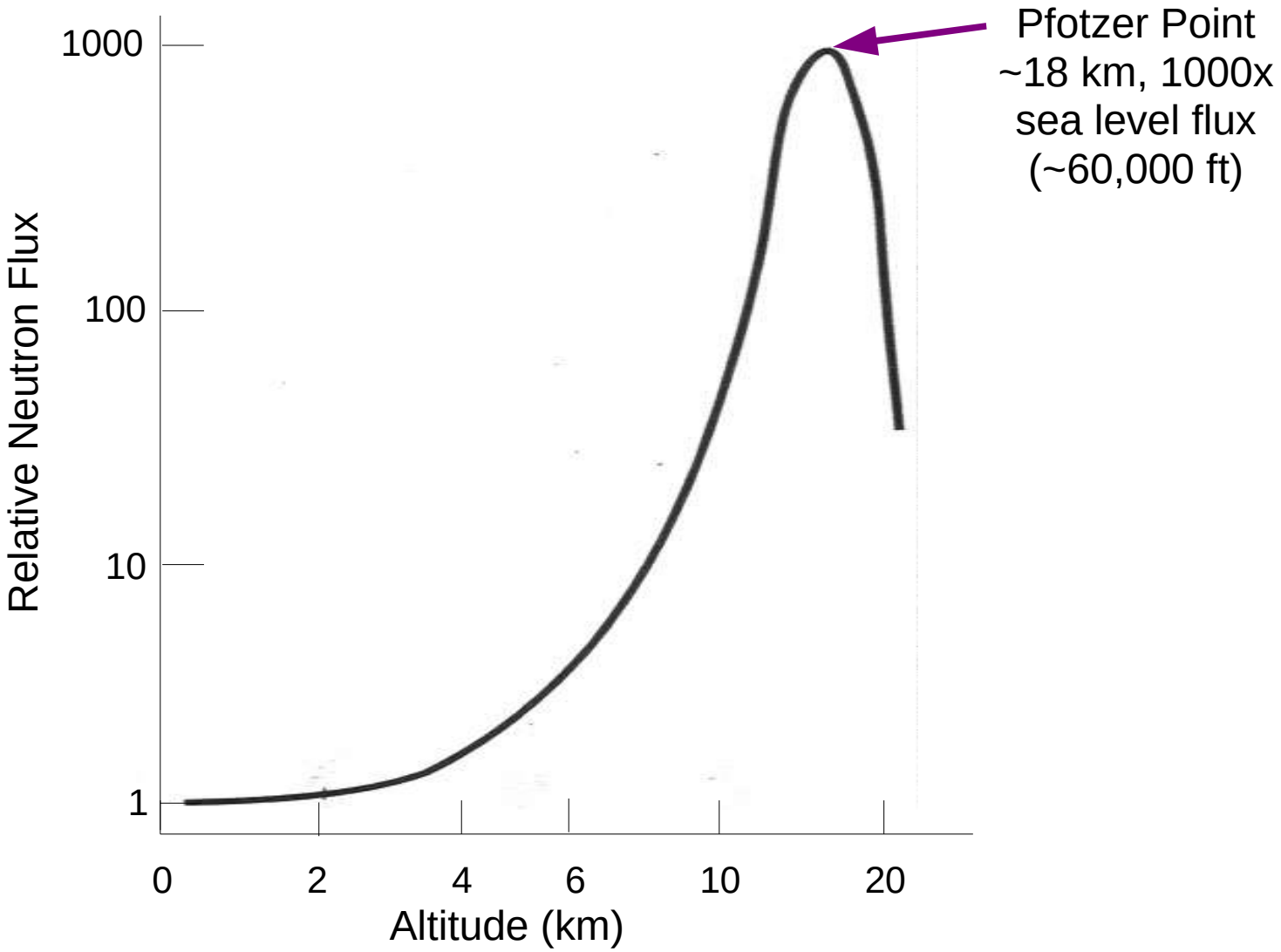
P. E. Dodd, et. al., "Production and Propagation of Single-Event Transients in High-Speed Digital Logic ICs," *IEEE Tran. Nuclear Science*, vol. 51, pp. 3278-3284, Dec. 2004.

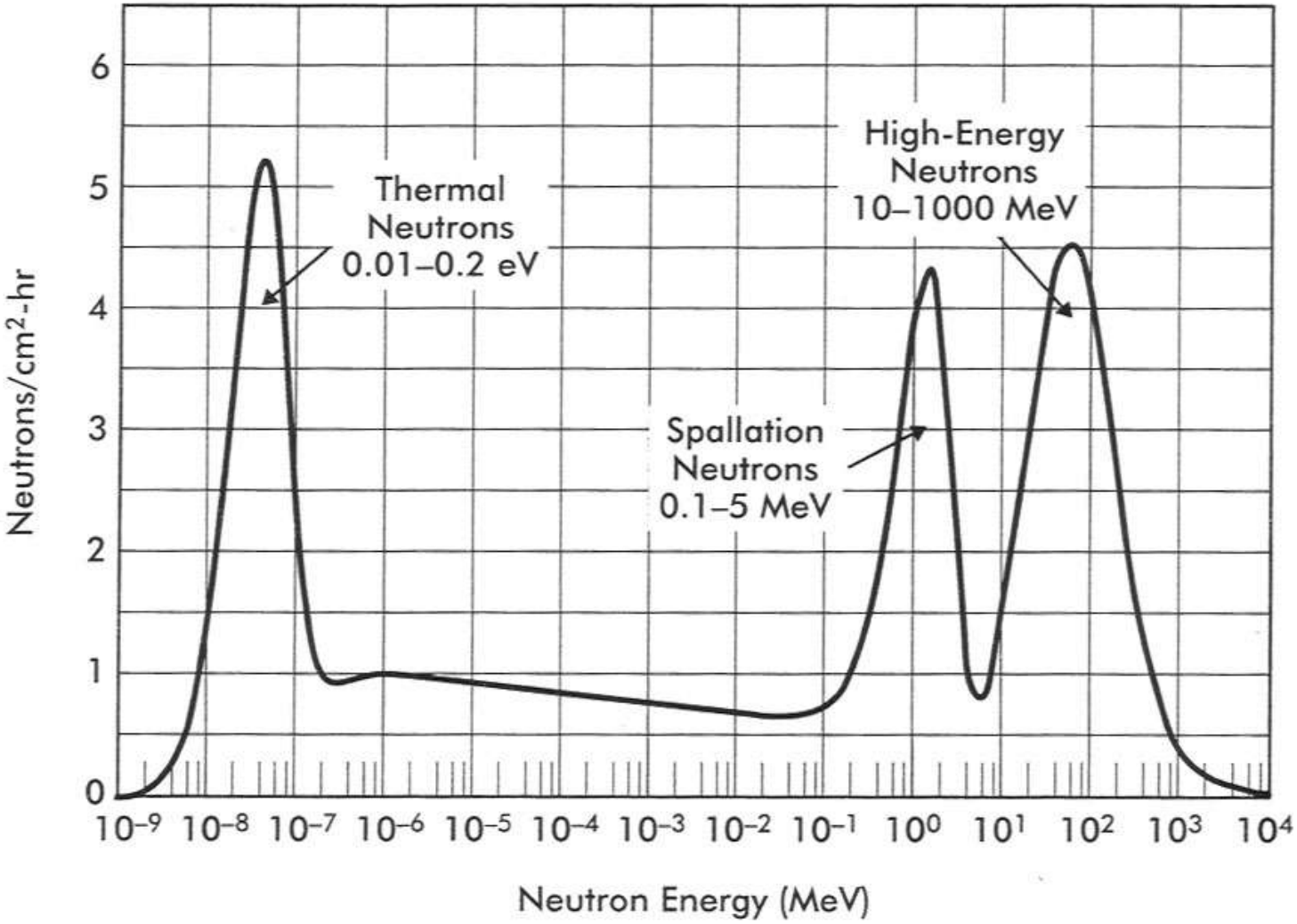
Backup Information

Neutron Flux with Altitude



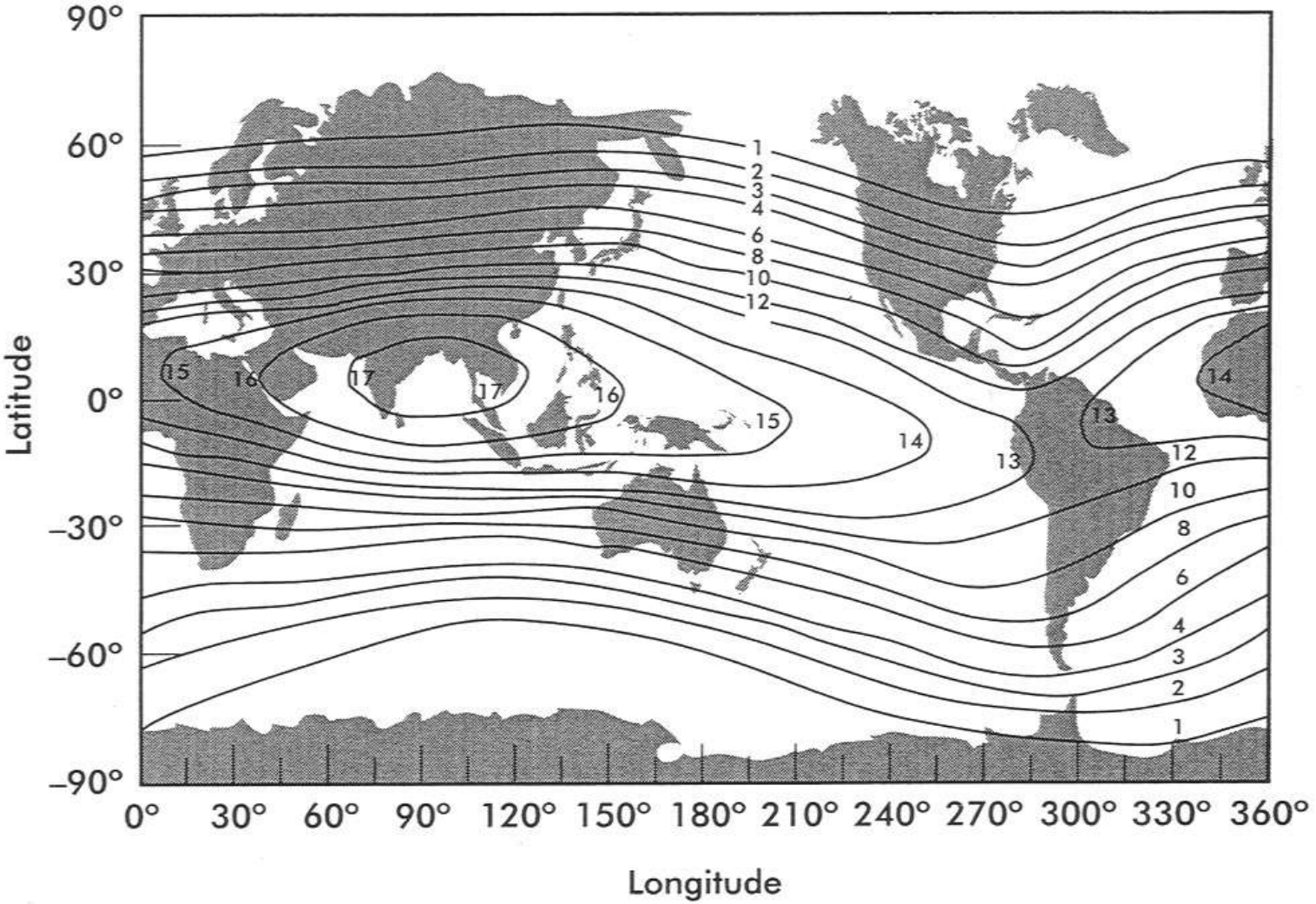
Ziegler & Puchner, Cypress Semiconductor [B].

Neutron Flux Energy Spectrum at Sea Level



Ziegler & Puchner, Cypress Semiconductor [B].

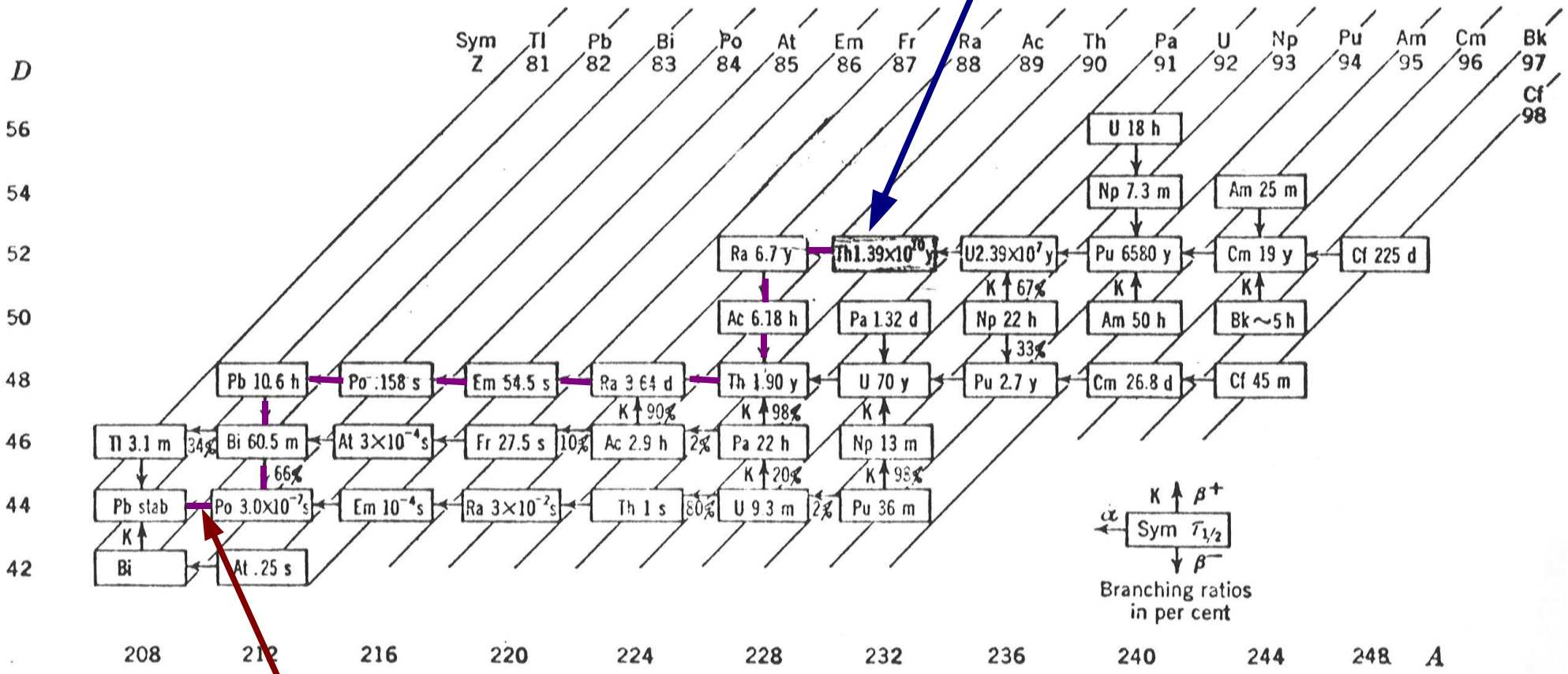
Geomagnetic Rigidity



Ziegler & Puchner, Cypress Semiconductor [B].

Heavy Metal Members of the 4n Radioactive Family

^{232}Th (1.39×10^{10} year half life)



$^{212}Po \Rightarrow {}^{208}Pb + 8.8MeV\ \alpha$

A. E. S. Green, *Nuclear Physics* [B].